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CHOPPER STABILIZATION TECHNIQUES. PART II: FREQUENCY SELECTIVE AMPLIFIER DESIGN

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Rezumat. *Lucrarea prezintă proiectarea optimală, bazată pe analiza manuală susţinută de simularea SPICE, a unui amplificator selectiv CMOS, privit ca bloc funcţional al unui amplificator cu modulare-demodulare (chopper). Avantajele folosirii ca amplificator de bază în cadrul unui amplificator cu chopper a unui amplificator selectiv în frecvenţă au fost puse în evidenţă în prima parte a lucrării, [1]. Cea de-a doua parte a lucrării este dedicată proiectării şi analizei amplificatorului de bază, care este un amplificator selectiv în frecvenţă de tipul g_mC. Sunt prezentate metoda de proiectare a amplificatorului selectiv g_mC şi rezultatele obţinute folosind un proces CMOS tipic de 0,6 µm. Modelul analitic al funcţiei de transfer a amplificatorului, dezvoltat şi folosit pentru analiza manuală, a fost validat prin compararea cu rezultatele obţinute prin simularea cu SPICE, diferenţele fiind mai mici de 20%*

Abstract. *This paper presents the chopper amplifier optimal design flow, based on manual analysis and backed up by SPICE simulation. The first part of the paper, [1], is a tutorial like overview of chopper technique effects on offset voltage and noise reduction, highlighting the significant results for the base amplifier design. The second part of the paper is focused to g_mC frequency selective base amplifier (FSA) design. An analytical model was developed for the FSA transfer function, and the results were checked versus SPICE simulation for a standard 0.6 µm CMOS process implementation, with less 20% error.*

Keywords: chopper amplifier, frequency selective amplifier

1. Introduction

The first part of this paper, [1], presented the chopper stabilization technique highlighting the advantages of using as a base amplifier a frequency selective amplifier (FSA). Chopper stabilization requires both signal *amplification* and *filtering*. An efficient solution is provided by the FSA use, as long as this amplifier combines these two functions. The second part of the paper is focused on the FSA design and performance analysis.

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For implementing a selective amplifier, a g_mC active filter topology was preferred, as it offers good performances at reasonable chip area in the desired frequency band. The FSA was implemented in a standard 0.6 µm CMOS process.

The *frequency selective base amplifier topology* has some important advantages over the wide band topology, [1]. Firstly, the residual offset voltage is significantly lower for a FSA topology, as it partially filters the spikes introduced by the square wave modulation process. These spikes are the main source of the residual offset. The FSA also provides an additional noise filtering that can improve noise performances. The 1/*f* noise corner frequency must be smaller than the modulation frequency, to reduce the total noise to the white noise floor level.

The *wide band base amplifier topology* offers both schematic simplicity and (ideally) a harmonic free output. For the FSA, the transfer function influences both signal distortions and noise and offset rejection. It is important to have a well designed transfer function, with constant gain and phase for the entire signal spectrum and high rejection outside the pass band. Also, the base amplifier pass band must be correlated with the modulation frequency.

As a symmetric modulating signal is used, for an asymmetric power supply system, a completely differential topology is required. This improves the common mode rejection and allows a higher signal variation. Overall, best performances can be achieved by using a FSA topology.

2. Frequency Selective Amplifier Design

2.1. Frequency Selective Amplifier Basic Schematic

This section presents a CMOS FSA implementation, based on g_mC techniques, intended for chopper stabilized amplifier use. The g_mC approach is largely used in present day IC design as it offers simple filtering and gain capabilities for a moderate frequency range at reasonable area consumption. The g_mC FSA are well suited for MOS technologies, where high input and output impedances can easily be achieved. Also, capacitors are quite easily implemented in MOS technologies.

The FSA presented in this section (see **Fig. 1**) is basically a parallel *RLC* resonator driven by a g_m stage [2], [4].

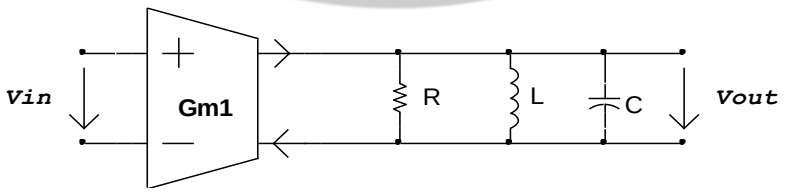


Fig. 1. FSA simplified schematic.

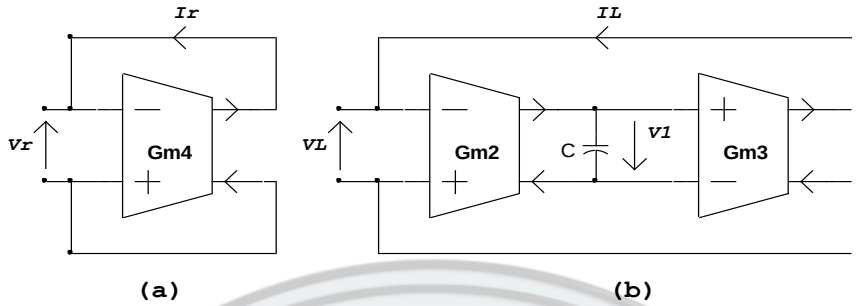


Fig. 2. Resistor, (a), and inductor implementation, (b).

Other g_m and g_mC stages are used to implement the resistor and inductor as shown in **Fig. 2**. The equivalent resistor and inductor equations are:

$$R_{\text{eq}} = \frac{1}{g_{m\text{S}4}}, \quad L_{\text{eq}} = \frac{C}{g_{m\text{S}2} g_{m\text{S}3}} \tag{1}$$

By replacing in **Fig. 1** the resistor and inductor by their g_mC equivalents from **Fig. 2**, we get the frequency selective amplifier functional blocks schematic, see Fig. 3. We note that this is a differential input, differential output amplifier. Such amplifier needs a common-mode feedback (CMFB) circuit to control the output voltages nodes and to force them to the desired value. The CMFB circuit will not be explicitly presented in this paper.

2.2. Frequency Selective Amplifier Transfer Function

In order to simplify the manual analysis, the g_m stages are modeled as ideal voltage controlled current sources. The FSA "ideal" transfer function results, [3]:

$$H_i(\text{j}\omega) = \frac{V_o}{V_i} = \frac{\text{j}\omega\, g_{m\text{S}1} / C}{(\text{j}\omega)^2 + \text{j}\omega\, g_{m\text{S}4} / C + g_{m\text{S}2} g_{m\text{S}3} / C^2}. \tag{2}$$

For a chopper stabilized amplifier, narrow bandwidth is needed in order to amplify the useful signal and to reject as much as possible the input noise.

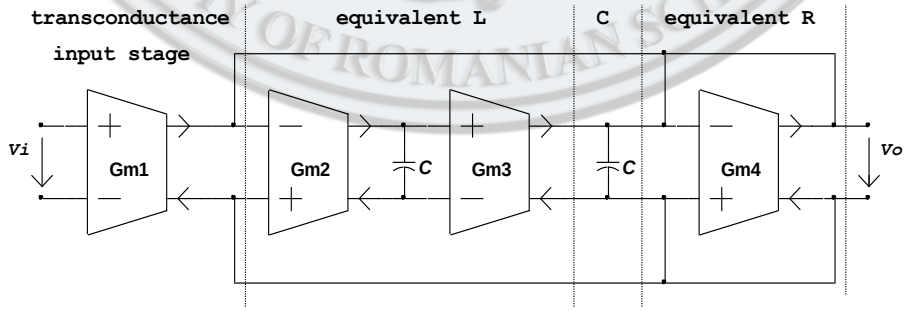


Fig. 3. FSA functional blocks schematic.

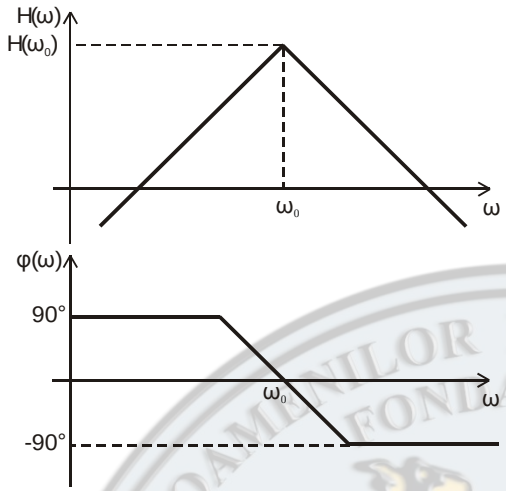


Fig. 4. FSA "ideal" transfer function.

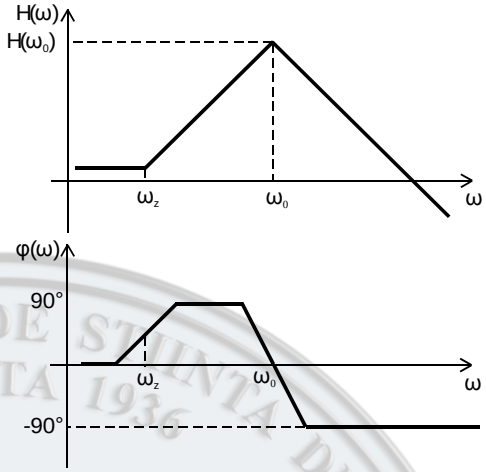


Fig. 5. FSA "real" transfer function.

To this end, we will consider a double pole transfer function. For a two poles transfer function, the narrowest bandwidth is reached when the two poles are overlapped. The condition to get a double pole transfer function is:

$$\Delta = g_{mS4}^2 C^2 - 4 g_{mS2}\, g_{mS3} C^2 = 0;\ g_{mS4}^2 = 4 g_{mS2}\, g_{ms3} \tag{3}$$

and the double root is given by

$$\omega_0 = g_{mS4} / 2C\,. \tag{4}$$

Replacing the double pole frequency [equation (4)] into the ideal transfer function [equation (2)] we get, [4]:

$$H_i(\mathrm{j}\omega) = \frac{g_{mS1}}{g_{mS4}} \frac{2\mathrm{j}\omega/\omega_0}{(1+\mathrm{j}\omega/\omega_0)^2}\,. \tag{5}$$

Fig. 4 shows the "ideal" transfer function Bode plots. This results support the *RLC* model. The total gain is determined by G_{m1} and the R resistor (implemented by G_{m4}). The gain magnitude peak equation is:

$$H_i(\omega_0) = g_{mS1} / g_{mS4}\,. \tag{6}$$

To accurately model the low frequency stage behavior, we must take into account the parasitic resistance effects. The only high impedance node is V_1 and we consider only its parasitic resistance, R_p. The "real" transfer function, results:

$$\frac{H(\mathrm{j}\omega)}{H_i(\omega_0)} = \frac{2\omega_0(\omega_z + \mathrm{j}\omega)}{(\mathrm{j}\omega)^2 + \mathrm{j}\omega(\omega_z + 2\omega_0) + 2\omega_0(\omega_z + 2\omega_0)}\,. \tag{7}$$

The zero frequency is now

$$\omega_z = 1/C\,R_p \tag{8}$$

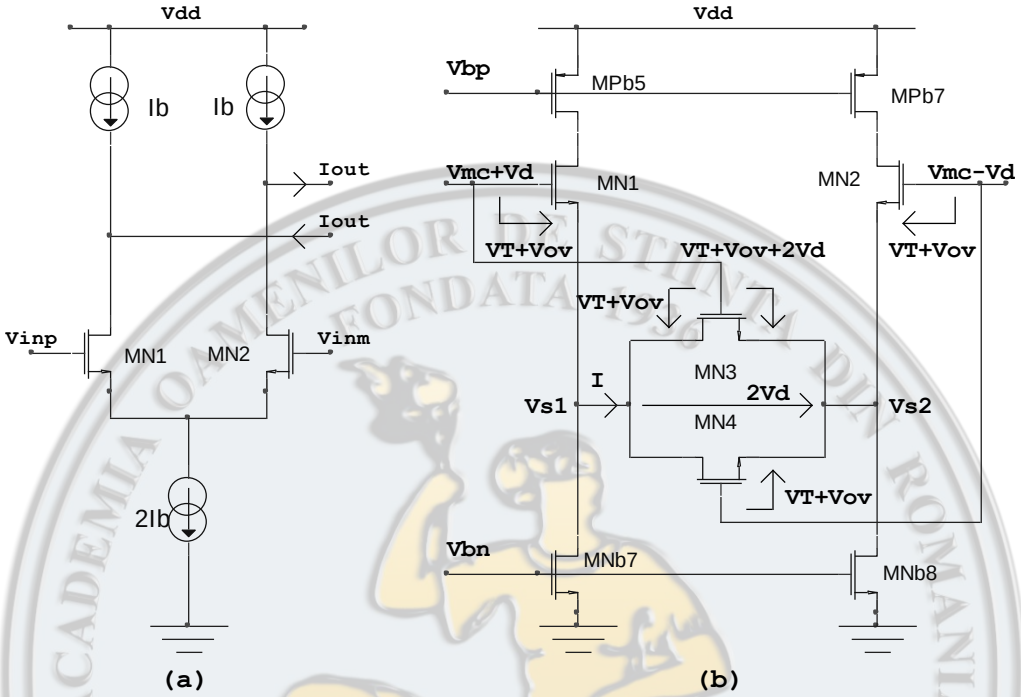


Fig. 6. (a) Standard differential pair and (b) Linearized g_m stage.

The transfer function's zero – see equation (7) – is no longer in origin but in ω_z. Fig. 5 shows the "real" transfer function Bode plots. The peak gain magnitude is also unaffected by R_p,

$$H(\omega_0)\big|_{\omega_z << \omega_0} \approx H_i(\omega_0). \tag{9}$$

2.3. Transconductance Stages

The gain magnitude peak is given by two stages g_m ratio [see equation (6)]. To get a large g_m ratio, we shall use two different g_m stage topologies: the standard differential pair and a linearized g_m stage. This technique allows getting a reasonable gain value, without unbalancing too much the two stages.

The standard differential pair transconductance stage is presented, [5], in Fig. 6.a and has a transconductance given by

$$g_{mS} = I_o / 2V_d = g_{m1}/2 = \mu C_{ox}(W/L)_1 V_{ov}. \tag{10}$$

A linearized g_m stage implementation using MOS transistors (instead of resistors) is presented, [6], in **Fig. 6**.b. The stage transconductance is given by:

$$g_m = I_o / 2V_d = 2\mu C_{ox}(W/L)_3 V_{ov} \tag{11}$$

For the standard differential pair, g_m is controlled by the differential transistors geometry [see equation (10)] while for the linearized transconductance stage, g_m is controlled by the MN3 and MN4 transistors geometry [see equation (11)]. This is an important difference between the two topologies, which allows getting a high g_m ratio for the two stages.

For transistors MP3 and MP4 we cannot discern between source and drain. If the input signal polarity changes, the source and drain change places. This is why we cannot connect MP3 and MP4 bulk to the source so we connect it to the highest potential, V_{dd}.

2.4. Frequency Selective Amplifier Design

Fig. 7 presents the frequency selective amplifier schematic, [2].

The input stage, G_{m1}, uses a standard differential pair, but the other stages use the linearized topology, to get a high g_{mS1}/g_{mS4} ratio[4]. In this case, the transconductance ratio, and thus the gain value, is controlled by the geometric ratio between the transconductances G_{m1} and G_{m4} of the stages differential pairs' aspect ratio. To keep the zero of the transfer function at low frequency were used the cascode current mirrors as they provide the high output impedance needed [see equation (8)].

The MP9–MP14 transistors have the bulk connected to V_{dda} as their source and drain are not predetermined. MP3–MP8 transistors also have their bulk connected to V_{dda} in order to have the same "substrate effect" and thus the same threshold voltage as MP9–MP14 transistors.

The frequency selective amplifier peak gain is given by equation (6). G_{m1} is a standard differential pair with the transconductance given by (10) and G_{m4} is a linearized g_m stage, with g_{mS4} given by (11).

We choose the same (W/L) ratio for all differential pairs (simple and linearized), so we have $(W/L)_1=(W/L)_4$. The gain peak value results, [4]:

$$H(\omega_0) = \frac{(W/L)_1}{(W/L)_9}\sqrt{\frac{I_{D1}}{I_{D4}}} \tag{12}$$

The bias currents values were choose I_{D1}=9 μA and I_{D4}=1 μA, and for all differential pairs were used L=10 μm, W=20 μm and m=4. For MP9 and MP10 transistors were choose L_9=10 μm and W_9=1 μm.

[4]The following notations are used: $g_{mS1\text{-}4}$ is the $G_{m1\text{-}4}$ stages transconductances and $g_{m1\text{-}4}$ are the MP1–MP4 transistors transconductances.

Based on these values the peak gain value results:

$$H(\omega_0) \cong 240 \tag{13}$$

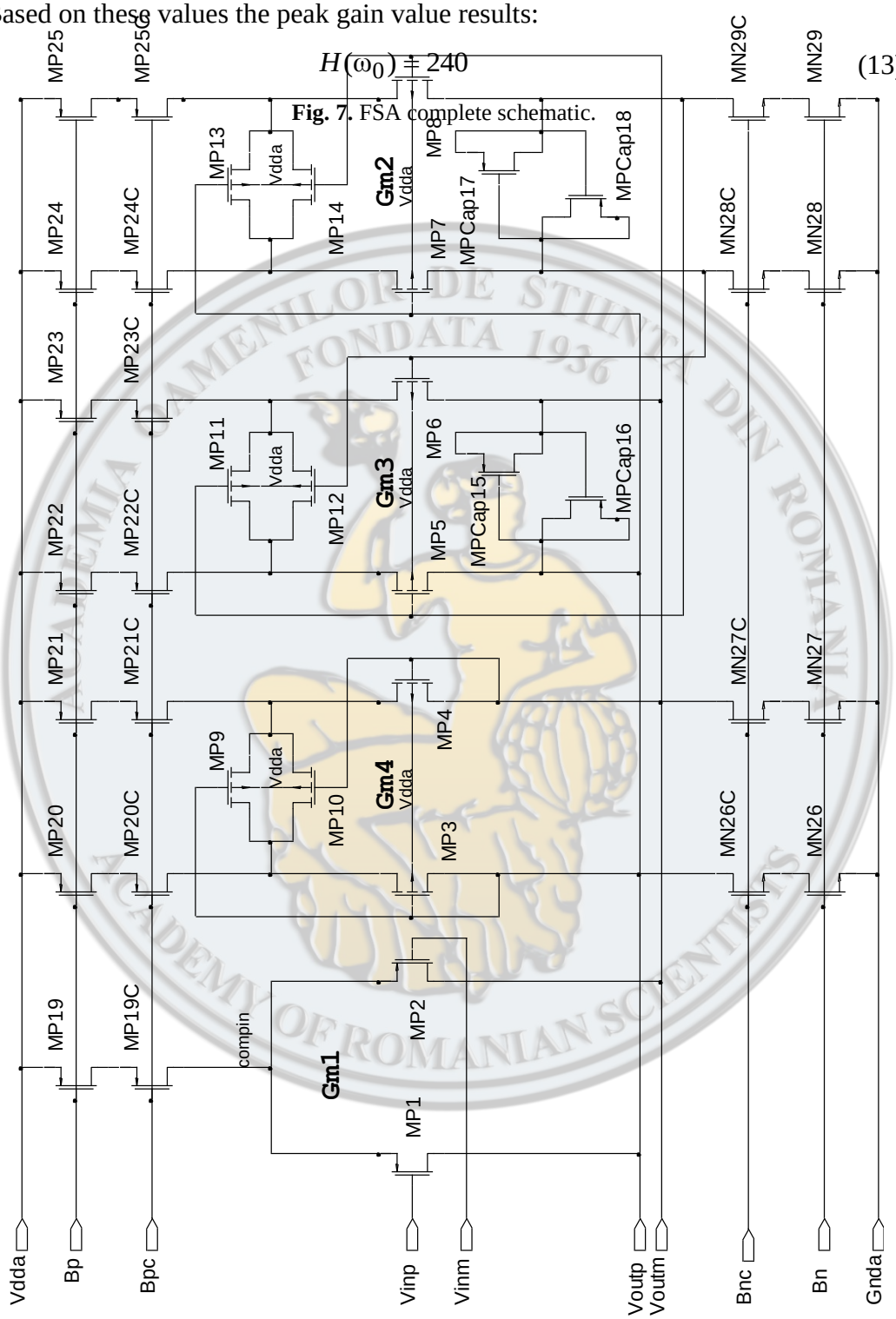


Fig. 7. FSA complete schematic.

The capacitance needed to get the desired resonance frequency results from equation (4) of the FSA double pole frequency:

$$C = \frac{g_{mS4}}{2\,\omega_0} = \frac{g_{mS4}}{4\pi\, f_0} \tag{14}$$

For a resonance frequency of f_0=10 kHz and for the transistor geometry given above, the compensation capacitor value is

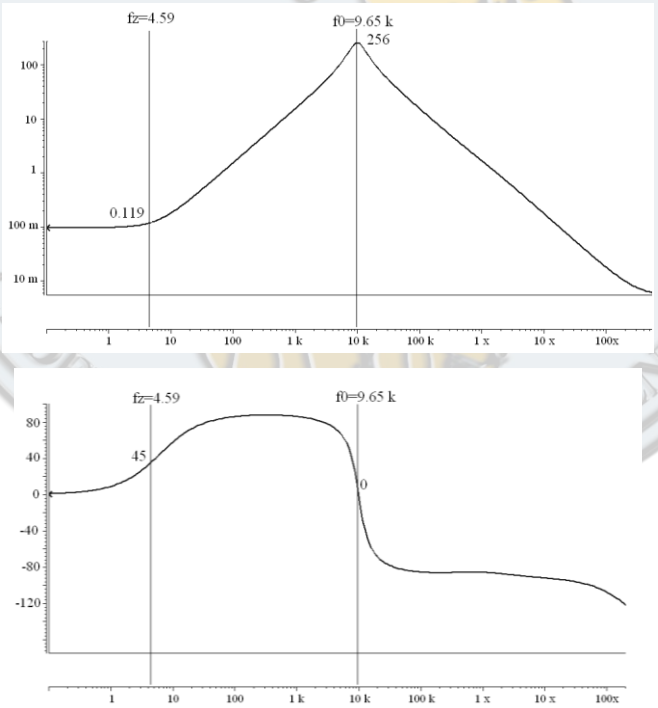
$$C = 2.16\,\text{pF} \tag{15}$$

that corresponds to a capacitor area of 1082 μm_2 (for C_{ox}=2 fF/μm^2).

This capacitor model does not take into consideration important parasitic effects, and we also neglected the differential pair's capacitance. This is why this area value has to be taken only as a first estimation and must be trimmed by several iterations using the SPICE analysis.

2.5. Frequency Selective Amplifier SPICE Analysis

The SPICE simulated, FSA transfer function's magnitude and phase is presented in **Fig. 8**. The resulted peak gain magnitude of 256 compares well to the manually estimated value of 240.



(a)

(b)

Fig. 8. SPICE simulated FSA transfer function: (a) magnitude and (b) phase.

The estimated capacitor area [see equation (14)] was used as a first iteration and the resulted resonance frequency was 14.8 kHz. Finally the capacitor area was adjusted to 1296 μm^2, in order to get the desired 10 kHz resonance frequency value.

The finite zero frequency (ω_z=4.59 Hz) introduced by the parasitic resistor is clearly visible in **Fig. 8**. We note that the $\omega_z << \omega_0$ condition is fulfilled and use ω_z to estimate the parasitic resistances, getting R_p=8 GΩ.

2.6. Selective Amplifier Peak Gain Analysis

The FSA gain peak value is given by equation (12). In this section, the transfer function manual analysis model accuracy versus the design parameters: $(W/L)_1$, $(W/L)_9$, I_{D1} and I_{D4} is checked using SPICE simulation. This analysis determines the peak gain changes versus process and bias variations

Firstly we consider the $H(\omega_0)$ versus $(W/L)_1$ dependency. The manual estimated and SPICE simulated $H(\omega_0)$ values are presented in **Fig. 9** showing a good agreement (relative error less than 20%) for $(W/L)_1$ values up to 15. For larger $(W/L)_1$ values the differential pair overdrive becomes very small, the transistor enters moderate and/or weak inversion region and the strong inversion model used in this paper to perform the manual analysis is no longer accurate.

The $H(\omega_0)$ versus $(W/L)_9$ dependency is presented in **Fig. 10**. The transistor width was kept constant, W_9=1 μm, and the transistor length, L_9, value was swept from 2 μm to 20 μm range, by 2 μm steps. Also were kept unchanged $(W/L)_1$=8, I_{D1}=9 μA and I_{D4}=1 μA. The $(W/L)_9$ ratio variation ranged from 0.5 to 0.05. The manual analysis results are in good agreement to SPICE simulation results over entire analyzed domain. $H(\omega_0)$ versus I_{D1} dependence is presented in **Fig. 11**. The following transistors' sizes and currents were used: $(W/L)_1$=8, $(W/L)_9$=0.1 and I_{D4}=1 μA.

The model is accurate at rather low currents. For larger currents values (in this case I_{D1} larger than 20 μA) SPICE simulation predicts a $H(\omega_0)$ saturation effect not predicted by the manual model.

The $H(\omega_0)$ versus I_{D4} is presented in **Fig. 12**. The following transistors' sizes and currents were used: $(W/L)_1$=8, $(W/L)_9$=0.1 and I_{D1}=9 μA.

It is worth to note that the FSA gain peak magnitude, $H(\omega_0)$, only depends on transistor geometry ratio and on bias currents ratio – it is independent of process parameters like μC_{ox} or transistors output resistance.

This fact explains the $H(\omega_0)$ manual evaluation accuracy. Indeed, SPICE simulation results differs no more than 20% from manual estimation results for a wide parameter range.

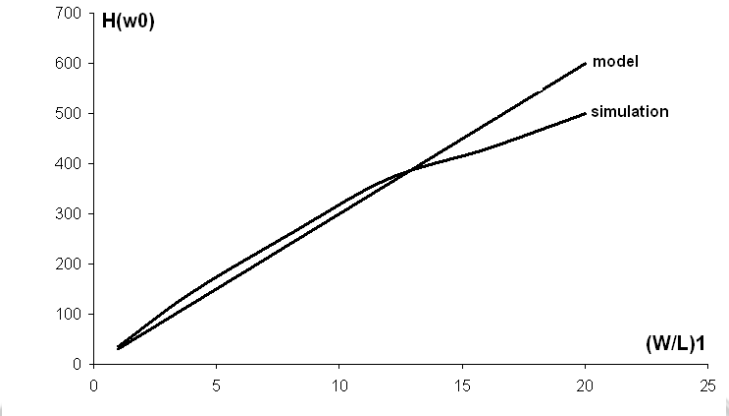


Fig. 9. $H\ (\omega_0) - (W/L)_1$ dependence.

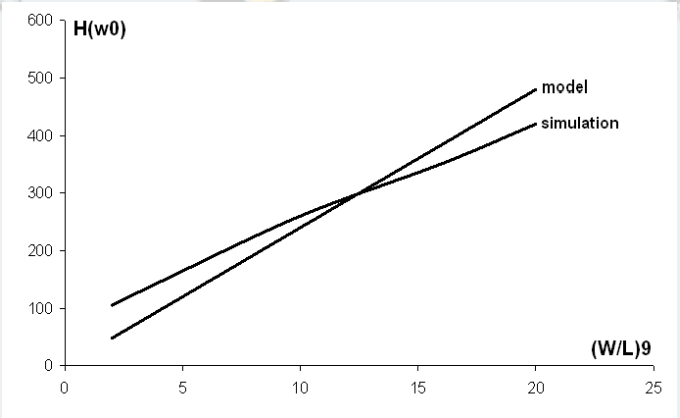


Fig. 10. $H\ (\omega_0) - (W/L)_9$ dependence.

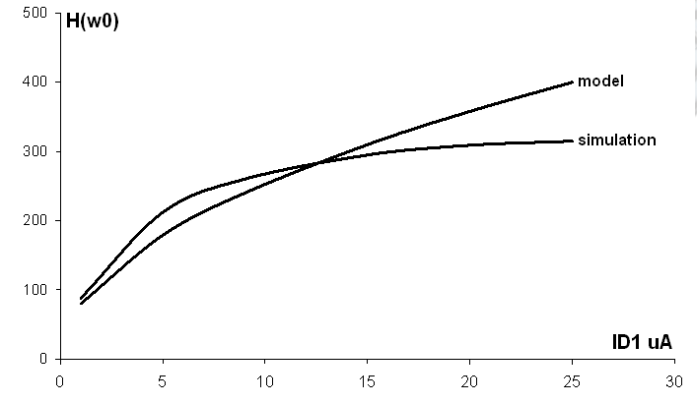


Fig. 11. $H\ (\omega_0) - I_{D1}$ dependence.

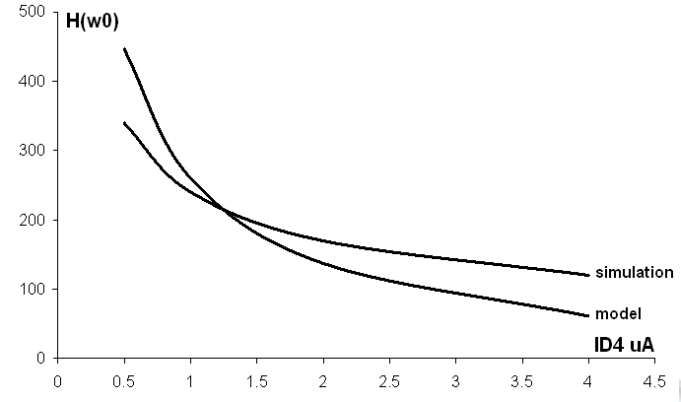


Fig. 12. $H(\omega_0) - I_{D4}$ dependence.

Conclusions

This paper presented the main design issues and an extended performance analysis of a frequency selective amplifier (FSA) intended for chopper stabilized amplifier use.

The FSA designed in this paper is based on an equivalent *RLC* parallel resonator, implemented using g_mC stages.

A simple model, suitable for manual analysis, of the FSA frequency behavior was developed: the FSA transfer function has a double pole at a design controlled frequency and a low frequency zero, which depends on the parasitic resistances of the high impedance node.

The peak gain value is determined by two transconductance stages g_m ratio.

In this paper, two different transconductance stage topologies were used: the simple differential pair and the linearized transconductance stage; in order to get a high g_m ratio.

Models suitable for manual analysis were presented for both topologies.

The manual estimation model results were backed up by SPICE simulation.

The amplifier designed in this paper has a resonating frequency of about 10 kHz with 256 gain peak value.

The manual analysis model validity of the gain peak value variation was validated by SPICE simulation.

The manual analysis results are in good agreement over a wide design parameters range with SPICE simulation results.

R E F E R E N C E S

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