The Early voltage was extracted from the output characteristics (Figs.6).

TABLE 1. Parameters extracted from the measured data for all studied devices

Parameter	**CMOS Process**					
	nMOS		***pMOS***			
L(μm)	1	0.35	1	0.35	0.18	0.18
W(μm)	25	0.5	25	0.5	2	0.4
$V_T(V)$	0.623	0.659	-0.7	-0.623	-1.42	-0.34
$k'(\mu A/V^2)$	160	210	45	60	116	100
$V_E(V)$	-353	-50.7	55.6	16.3	–	–
$a^*\zeta_c(V/\mu m)$	1.74	1.22	3	3	3	3

A complete strong inversion plot for the output characteristic of a *1*μm channel *n*MOS device is shown in Fig.7.

As we have seen earlier, the active region measurements agree completely with the model. Still, when considering the triode region, a noticeable overestimation of the real current in the channel is obtained with the model.

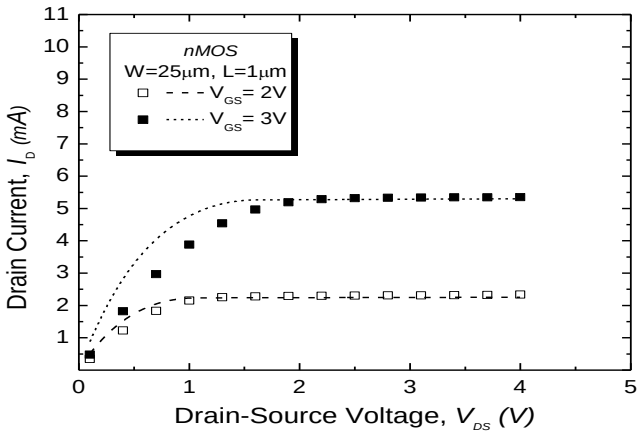
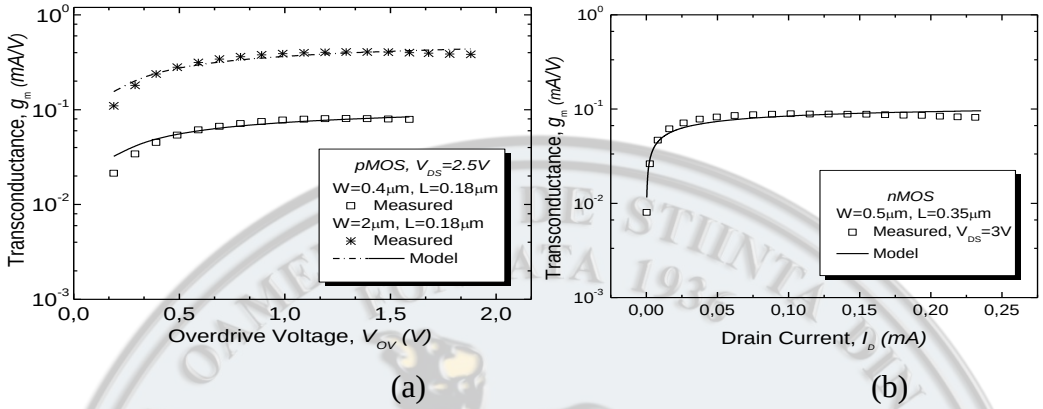


Fig.7. Complete strong inversion plot for drain current as a function of V_{DS} for an nMOS transistor

This difference, which increases at higher gate voltage (Fig.7), arises from the modulation of the carrier mobility in the channel.

Due to the high electrical fields created by the gate biasing the carrier mobility is additionaly reduced determining an increase of the importance velocity saturation effect. This fact shows the importance of the inclusion of velocity saturation in any analytical model for the MOSFET.

The transconductance curves calculated using (16) are compared with the experimental data in Figs.8. The same good theory – experiment agreement as for the transfer characteristics (Figs. 5) is obtained, for any channel width (Figs.8).



(a) (b)

Fig.8. Transconductance dependence on drain current for: (a) pMOS; (b) and (c) nMOS

6. Conclusions

An accurate analytical model with a reduced parameter set for submicron MOS transistors was presented.

The model takes into account the velocity saturation in the channel and the channel-length modulation.

Simple equations with just a few parameters were obtained for the drain current, drain voltage and transconductance for both *p*MOS and *n*MOS transistors.

For *n*MOS transistors, a linearization of the carrier velocity dependence on the longitudinal electrical field was necessary.

Several new parameters were introduced in the model in order to evince the velocity saturation importance.

The knee point corresponds to the bias which creates the critical eletrical field.

For biasing over the knee point the velocity saturation effect becomes predominant.

A new expression of the drain current, which takes into account the channel length modulation, was achieved.

A new expression of the drain current in the active region, which takes into account the channel-length modulation, was obtained.

This equation evinces that the drain current increases due to the voltage drop on the effective pinch-off region.

The accuracy of the proposed model was proven by comparing it with the experimental data measured on *p*MOS and *n*MOS transistors fabricated in the standard 0.18, 0.35 and 1 μm CMOS processes.

A very good theory-experiment agreement was obtained for the transfer characteristics, output characteristics and the transconductance.

It was demonstrated that the model correctly predicts the significant effect of the carrier velocity saturation on several analogue parameters of the MOS transistor.

The model, being based on a reduced set of parameters, can be easily implemented in an analogue ICs simulator.

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