ANALOG SWITCHES BASED ON MOS TRANSISTORS IN SUB-MICRON TECHNOLOGIES

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Abstract. *This paper is meant to present a study of MOS transistors usage in analog switches integrated circuits. MOS transistors' parameters, technology factors and topologies for switches are presented, based on the literature synthesis. The study continues by exposing a few improved switches architectures and their migration in sub-micron process technologies. These are part of the preliminary accomplishments of the first author's PhD thesis.*

Keywords: analog switches, MOS transistors, serial controller, sub-micron CMOS process

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1. Introduction

Nowadays technological advancements are possible due to the extraordinary developments in the fields of electronics and microelectronics. These industries' evolution was determined by the continuous progress in manufacturing CMOS technologies, stringent requirements of recent applications and design of up-to-date mixed signal circuits architectures. Sub-micron CMOS process technologies brought cost reduction of complex architectures [1]. Mixed signal integrated circuits are extensively designed, implemented and sold for satisfying tight requirements enabling easier integration in embedded systems.

Digitally controlled, analog switches represent a category of mixed signal circuits widely used in the automotive and aviation industries, in test, control equipments, in signal processing systems, etc [2-3].

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This paper starts with an extensive study of MOS devices in switches configurations. It continues with an analysis of improved architectures for switches meant to better integrate them in complex applications [4-8]. There are emphasized the advantages of digitally controlled analog switches using serial interfaces. Concretely, we focused on the design of multichannel switches, enabled or disabled by digital control blocks. The internal structures, main electrical parameters and layout designed for implementation are displayed. The validation of these architectures was done by digital and transistor-level simulations, static time analysis and noise studies. We will introduce the present results on an 8-channel system whose operating frequency was increased from 2.5 MHz [6] to a 55 MHz clock signal, in the context of insignificant deviations from logic levels [7].

The paper is structured as follows: section 2 offers an analysis of main parameters and characteristics of MOS transistors used for switches, sections 3 and 4 reveals the directions in improved topologies of switches and finally, the conclusions are drawn.

2. MOS devices operation as switches

Extensive usage of MOS transistors in mixed signal circuits was due to their advantageous features like good operation as switch, reduced parasitic elements, improved density integration and straightforward manufacturing process [9].

In Figure 1 is depicted the transversal section of CMOS cell. P-channel transistor is formed by two doped p+ regions in a slightly n doped material– known as well. These two regions correspond to source and drain, and they are separated by a distance, L, denoting the length of the device. Between the source and drain there is the gate electrode, separated by Si through an oxide, SiO2. In a similar way, the NMOS device is built [10]. The contact for bulk or substrate is common for the entire circuit and it is connected to ground. In some situations, we may have several wells, individually connected to any potential – forming isolated devices (Figure 1). The aspect ratio - $\frac{W}{L}$ (where W – width and L – length) is the most important parameter of the transistor since the current is proportional with it.

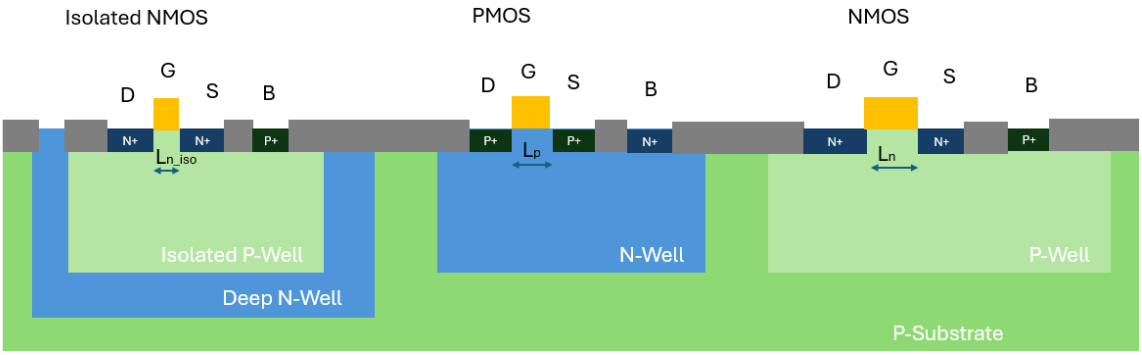

Fig. 1. Transversal section of CMOS process with isolated NMOS device

Another important parameter is the threshold voltage setting the limit between cutoff and conduction, being dependent on the bulk bias.

$$V_T = V_{T_0} + \gamma(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{2\phi_F}) \quad (1)$$

In (1), with ϕ_F was noted the Fermi potential, with γ - the body effect coefficient and with V_{SB} - the source-bulk potential difference.
MOS devices have three operation regions: cut-off, linear and saturation. Switch-like operation corresponds to the linear regime. For an NMOS device the conditions in (2) and (3) had to be fulfilled for operating in linear region.

$$V_{GS} > V_T \quad (2)$$

$$V_{DS} < (V_{GS} - V_T) \quad (3)$$

For a complete input range [0 - V_{DD}], a standalone NMOS transistor, activated with a voltage gate of V_{DD} is able to pass voltages applied on source to the drain until it reaches $V_{DD} - V_T$. On the other way, the PMOS device will pass only voltages greater than V_T.
On resistance formula for a transistor is noted down.

$$R_{ON} = \frac{1}{\frac{\vartheta I_D}{\vartheta V_{DS}}} = \frac{L}{K'W(V_{GS} - V_T)} \quad (4)$$

To pass the entire signal, a transmission gate topology must be used, where a NMOS and a PMOS devices have the interchangeable source/drain terminals connected and the gates in $V_{DD}$for NMOS and 0 for PMOS (Figure 2).

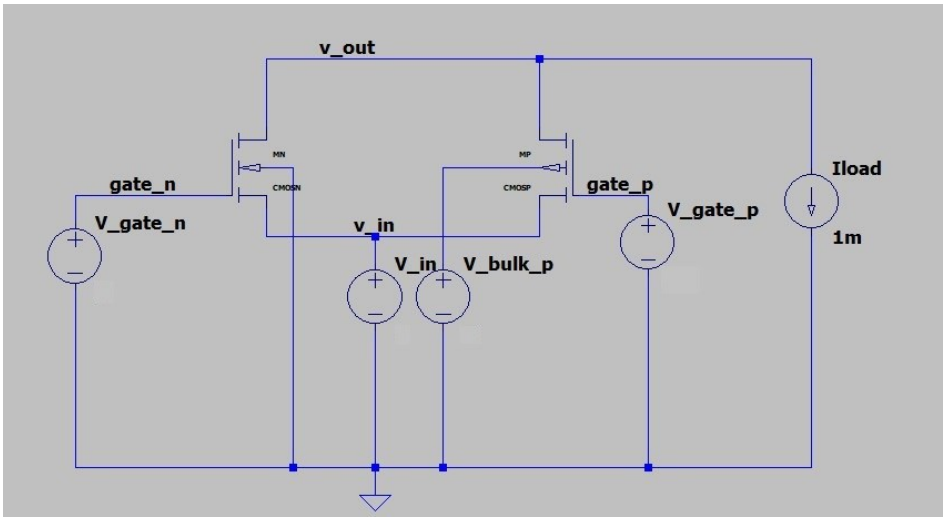

Fig. 2. Transmission gate configuration

In Fig. 3 the waveforms corresponding to the drain currents of the transistors and the RON graph for a sweep of the input voltage (v_in) is showed. The transmission gate resistance is computed according to:

$$R_{ON} = \frac{v\_in - v\_out}{iload} \tag{5}$$

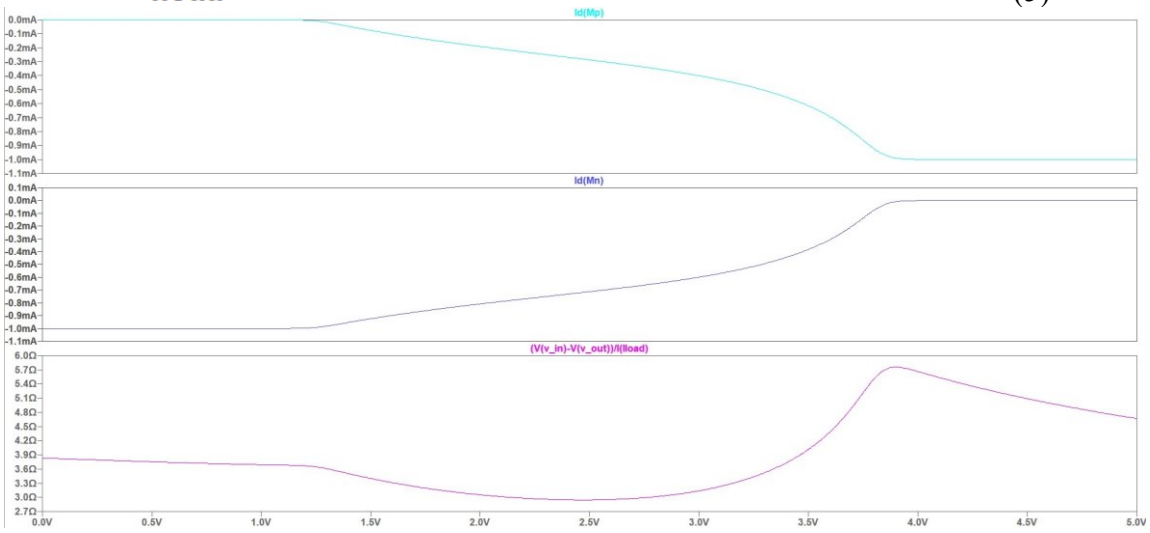

Fig. 3. Simulation waveforms: a) Id PMOS b) Id NMOS c) Ron

We can see that for lower voltages, PMOS is off (Id ~0) and the NMOS drain conducts the 1mA current load. From ~1V until ~(V_{DD} -1V) both transistors are ON, and we can observe the pronounced liniar slopes of the currents. From 4V, the PMOS is only ON (NMOS is OFF) and conducts the load current (1mA). The

bulks of the transistors are fixed in 0V for NMOS and 5V (VDD) for PMOS. Since the voltages applied as v_in is varying from 0 to 5V, both transistors suffer from the source-bulk difference effect which increases the absolute value of the threshold (2). ON resistance graph was computed with (5) and we can observe that from 0 to V_{DD} is given by the NMOS resistance, from ~(V_{DD} -1V) to V_{DD} is given by PMOS resistance and in between these intervals is the paralel equivalent of the NMOS and PMOS resistances.

3. Switches with improved overdrive voltage

Analog switches are integrated circuits based on transmission gates able to bilaterally transmit analog signals varying from 0 V up to V_{DD}. Their integration in complex embedded systems is conditioned by some requirements like transmission paths with small delays, digital activation/deactivation and low distortions.

The interest in designing analog switches architectures is active, proved by different directions meant to bring improvements of the classical topology based on transmission gate (Fig. 2).

One direction of improving the switches was the insertion of charge pump circuit meant to ensure bigger overdrive, $V_{GS} - V_T$, limited by the breakdown voltage of the gate oxide of the switch. The charge pump will be supplied from the system supply – a lower voltage and will produce a stable and greater voltage which will be applied on the gate of the NMOS transistor used in the switch. Increasing the overdrive voltage, the ON resistance will be decreased.

In [5] there is presented a charge pump architecture designed to ensure a DC output voltage of typical 5 V when the input voltage is ranging from 2.7 V to 3.3 V. The diagram of the charge pump is depicted in Figure 4.

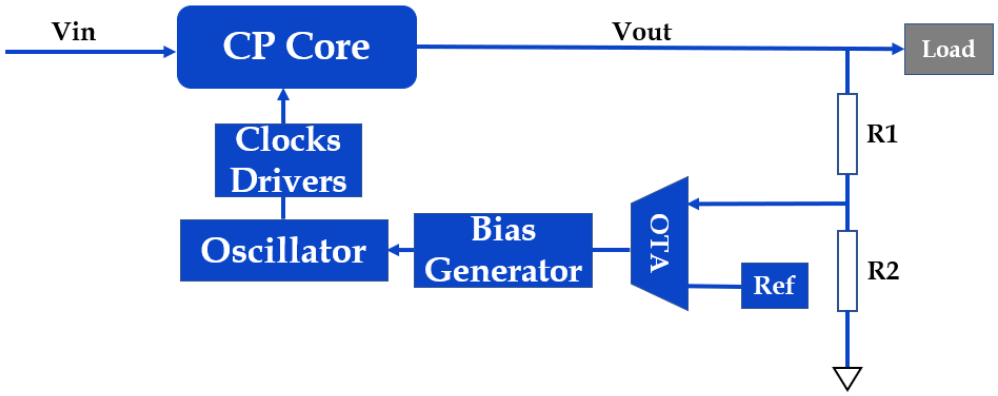

Fig. 4. Charge pump internal architecture [5]

The price for integrating charge pumps to ensure better overdrive to the switch are the increased area and the increased complexity of the driving circuit.

4. Digitally controlled switches

The analog switches require an individual control signal [11] or may require some multiplexer mechanism [12]. For systems based on multiple transmission channels, now there are tendencies to ensure the control of activating a certain number of channels in a synchronous way by usage of serial interfaces compatible with SPI (Serial Peripheral Interface) or I2C (Inter-Integrated) protocols.

In [6] we present a multi-channel switch containing eight transmission gates whose activation is controlled by the value written in the internal register of the digital interface (Fig. 5). This register is written or read by SPI commands. This was able to work with voltages ranging from 3.0 V to 5.5 V with frequencies up to 2.5MHz. Regarding the digital interface the circuit was able to work on entire targeted PVT space with at 10 ns setup time and with a hold time as small as 0 ns [6]. For RON resistance, values around 120 Ω are obtained at 5V supply, at 25ºC. The enable/disable times are no larger than 29 ns [6].

The serial controller presented in [6] was re-designed to operate at higher frequencies up to 55 MHz, for supply voltages between 2.5 – 5.5 V [7], [8]. Also, for this circuit the serial controller architecture was upgraded for a more complex functionality involving addition of power-on-reset input, increasing the number of store register from one to five and addition to a configuration register for software reset command [7], [8].

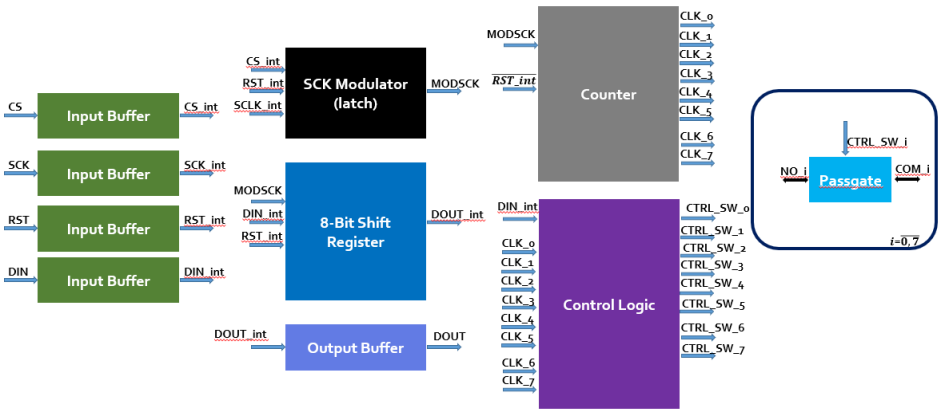

Fig. 5. Multi-channel switch with SPI controller [6]

Figure 6 depicts the diagram of the second implementation of the serial control block. Among typical SPI pins, PORB - Power-on-Reset input, we have also Q [7:0] – eight parallel outputs meant to enable/disable up to eight switch channels [5], [6].

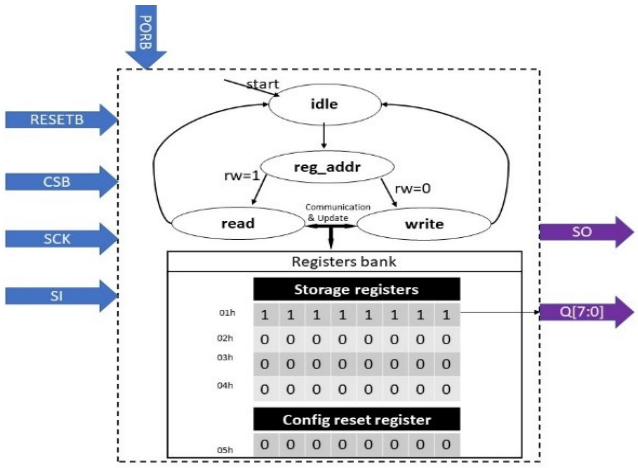

Fig. 6. Concept diagram for second implementation of the SPI block [5]

The main internal structures of the circuits depicted in Figure 6 are the finite state machine which decode the instructions and delivers internal control signals to renew the content of the registers bank, logic for latching and storing the default output code for serial output, bits counter, four storage registers - register located at address 0x01 activates the switches) and a reset register. This circuit is conformable to Mode 0 SPI protocol [7], [8].

The schematic and layout of this circuit was done in a CMOS 180 nm technology. The proposed schematic obtained by means of digital synthesis was validated by post layout simulations to work with frequencies up to 55 MHz, with voltages between 2.5 V ÷ 5.5 V. Timing analysis also confirmed the timing performance for clock signals period of 18 ns. The sequential chains were designed to maintain positive values for setup and hold parameters. The ability to operate at very high frequencies was due to usage of logic cells with small propagation delays [5], [6]. Proper operation at high frequencies without timing violations was also possible due to the synthesis of the clock tree configuration. Its purpose is to dispense the clock signal uniformly to all leaf cells, to minimize propagation delays and skews [5], [6].

Conclusions

A review of the analog switches' construction, parameters and challenges were listed. A charge pump architecture which can provide a **5V DC** voltage useful for ensuring better overdrive for switches is shown. The first multi-channel SPI circuit is presented able to work with **2.5MHz** at **3.0-5.5V**. The second architecture contains a more complex digital architecture able to operate at **55 MHz** for voltages from **2.5V** to **5.5 V**. The increase of the operating frequency is

one of the consequences of improvement of the manufacturing processes and shrinking of the transistors' geometry.

REFERENCES

[1] T. Hiramoto, *Never-Ending CMOS Innovation: The Past, Present, and Future Perspectives*, 2020 International Symposium on VLSI Technology, Systems and Applications, 2020, Hsinchu, Taiwan, pp. 3-4.

[2] *Selecting the Right CMOS Analog Switch*, web page's address https://www.analog.com/en/resources/design-notes/selecting-the-right-cmos-analog-switch.html

[3] *SN74HC4066 Quadruple Bilateral Analog Switch*, web page's address https://www.ti.com/lit/ds/symlink/sn74hc4066.pdf

[4] G. Brezeanu, I.-B. Brezeanu, *Increasing the Performance of Analog Switches Controlled Through Serial Interfaces*, National Scientific Conference Academy of Romania Scientists, Book Of Abstracts (Bucharest, Romania, 2024) Volume 18, issue 1, 2024, ISSN 2601-5102, https://www.aosr.ro/wp-content/uploads/2024/05/VOLUM-DE-REZUMATE-PRIMAVARA-2024-SITE-1.pdf.

[5] Ionelia-Bianca Brezeanu, Cătălin Botezatu, Alexandru Vasile, Gheorghe Brezeanu, *The Impact of the Sub-circuits Parameters on the Efficiency of a Charge Pump*, 2021 IEEE 27th International Symposium for Design and Technology in Electronic Packaging (SIITME), Timișoara, Romania, 2021, ISBN: 978-1-6654-2110-2, WOS: 000786441900057

[6] Ionelia-Bianca Brezeanu, Cătălin Botezatu, Florin Drăghici, Gheorghe Brezeanu, *Improved SPI Controlled, Low-Voltage, High Speed, Multi-Channel Switch*, 2022 14th International Conference on Electronics, Computers and Artificial Intelligence (ECAI), Ploiești, Romania, 2022, ISBN: 978-1-6654-9535-6, INSPEC Accession Number: 21990215

[7] Ionelia-Bianca Brezeanu, Silviu Isari, Alexandru Vasile, Gheorghe Brezeanu, *Design and Verification of a High Frequency, SPI Control Block*, 2023 International Semiconductor Conference (CAS), Sinaia, Romania, 2023, ISBN: 979-8-3503-2396-2

[8] Ionelia-Bianca Brezeanu, Silviu Isari, Gheorghe Brezeanu, *Improved Serial Peripheral Interface Controller Based on Scan Architecture*, ROMJIST, Vol. 27, No. 2, 2024.

[9] J. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits – A design Perspective, Lectures Slides, 2002.

[10] B. Razavi, *Design of Analog CMOS Integrated Circuits* (McGraw-Hill Series in Electrical and Computing Engineering, New York, USA), 2001.

[11] *2-channel general-purpose analog switch with low on-state resistance – Texas Instruments,* web page's address https://www.ti.com/product/SN74LVC2G66 .

[12] *Analog Multiplexer Demultiplexer,* web page's address https://www.onsemi.com/pdf/datasheet/mc74lvx4051-d.pdf.