SIMULATION TECHNOLOGIES USED IN HIGH-SPEED PRINTED CIRCUIT BOARD DESIGN

Sorin BURDUCEA[1], Miron ZAPCIU[2]

Rezumat. *Proiectarea circuitelor imprimate și a chip-urilor moderne implică lucrul cu fronturi de undă extrem de rapide, care generează o gamă largă de armonici superioare. Acestea schimbă distribuția curenților electrici, generând interferențe electromagnetice, cuplarea între liniile adiacente, dezechilibrul sistemului de alimentare, reflexii, rezonanțe și efecte termice nedorite. Utilizarea instrumentelor de simulare și gestionare a constrângerilor sistemului electronic este absolut necesară, iar progresul tehnologic din ultima perioadă a adus cu sine o gamă de algoritmi capabili să anticipeze în proporție semnificativă funcționarea dispozitivelor electronice.*

Abstract. *Fast transients of today's chips generate a large amount of high frequencies harmonics which in turn bring upon the designer an increasing amount of problems. Heat, crosstalk, electro-magnetic interference, ground bounce, reflections, plane resonance and many other issues turn the design decision making into an extremely complex problem. The use of tools for simulating and managing the constraints of the electronic system is absolutely necessary, and recent technological progress has brought with it a range of algorithms capable of significantly anticipating the operation process of electronic devices.*

Keywords: Simulation, PCB, Heat management

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1. Introduction

The scope of this paper is to set the grounds for a hardware solution on which the open ODrive servo motor control firmware can be implemented. The emphasis is on PCB design. This work presents the placement of the components on the PCB, based on their thermal footprint and electronic schematic. For simulation purposes, Ansys IcePak will be used.

Electronic layout of servomotor

The electronic schematic is being developed first. The design draws on component manufacturer application notes and on ODrive's 3.5 schematic. There are however significant differences from ODrive schematic regarding the brake chopper schematic, power distribution, absence of CAN bus and IO header layout. In order to organize the electronic components, they were grouped together

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around their corresponding *Integrated Circuit*. This makes the placement faster and more comprehensive. The rules of placement are based on maximizing cooling effect, minimizing tracks length and crossing, efficient power distribution and minimizing PCB area. After the initial placement, the components may be repositioned as to minimize crosstalk and EMI effects. As these effects may only be determined after placement, repositioning is inevitable, making the process an iterative one. Along the way, the initial solution may change as more insight is gained during simulations and analysis.

2. Components thermal characterization

Thermal effects have an outstanding impact on electronics performance. Careful judgement of PCB layout is critical. Components with high power dissipation must be identified, their power loss must be quantified and based on a set of rules, a way to dissipate the generated heat into the surrounding environment needs to be found.

Every IC component on the board makes a good candidate for thermal analysis along with some passive components that are part of the power stage:

- STM32F405 microcontroller
- Both DRV8301 three phase drivers
- AZ1117EH-3.3 low dropout regulator
- 2mOhm current sense resistors
- Bulk power stage capacitors
- MOSFET transistors

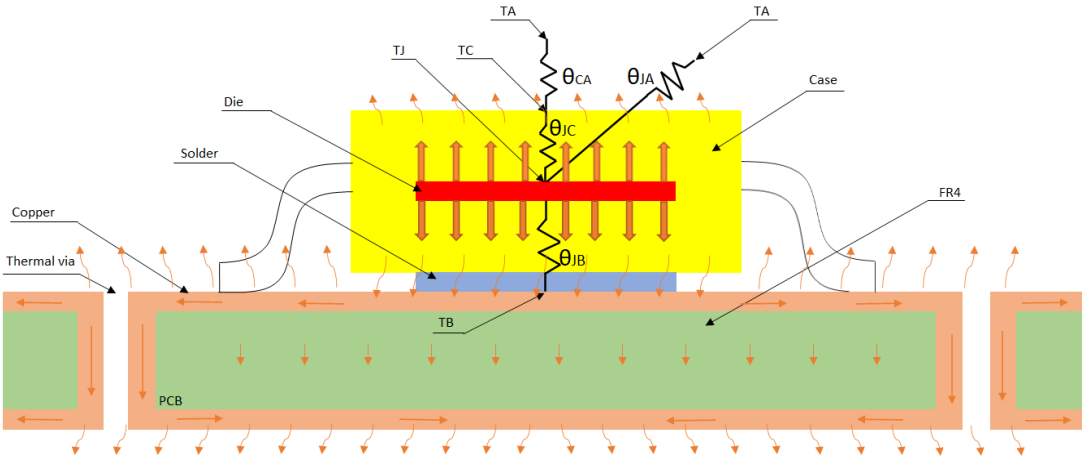


Fig. 1. SMD component thermal characterization

Thermal characteristic of the components is mainly described by the thermal resistances found within them and at junction layers. Primarily they are θ_{JC} - thermal resistance between the die and the package (case), θ_{CA} - thermal resistance between the package and the air surrounding the package, θ_{JB} - thermal resistance between the die and the PCB on which the IC is mounted on, θ_{JA} - thermal resistance between the die and the air surrounding the die package (Fig. 1). The temperatures of interest are TJ – junction temperature, TC – package temperature, TA – ambient temperature (air surrounding the package), TB – board temperature near the package.

At the heart of any thermal characterization lies the junction temperature TJ. It describes the array of temperatures and gradients that the die is experiencing during operation. Almost all electrical parameters of the device are impacted by it. One of the most important parameters that are greatly influenced being no other than the device reliability itself. In PCB layout practice, the die temperature is theoretically considered to be uniformly distributed and therefore a single value is normally found in the vast majority of the cases. For larger components with relatively high gradients, this may be of concern. Luckily, the components used within this work approximate well to a uniform distribution and no concern needs to be raised.

Case temperature is the temperature that is measured on the top of the device. Based on this temperature, in the absence of a die integrated measurement, the junction temperature can be derived. Board temperature is from the practical perspective of primordial importance since the heat dissipation in most cases takes the route towards the PCB. The board temperature TB alongside the package Theta – JB (junction-to-board) thermal resistance are the parameters used when assessing the device thermal performance.

STM32F405 has according to its datasheet [1] a P_D (maximum power dissipation) of 435mW and a maximum junction temperature T_J of just 105degC. Giving the low junction temperature, the microcontroller will have to be placed at a safe distance from the high temperature devices like MOSFETS. In order to understand the amount of PCB area that will be required to keep the device at a safe temperature below 80degC, Ansys IcePak will be used to simulate a double sided FR4 PCB, with 1 oz. thick copper layers and 50% copper on both sides to compensate for the tracks under and around the chip (Fig. 2).

The simulation was conducted considering an ambient temperature of 25degC and the air movement was only due to natural convection.

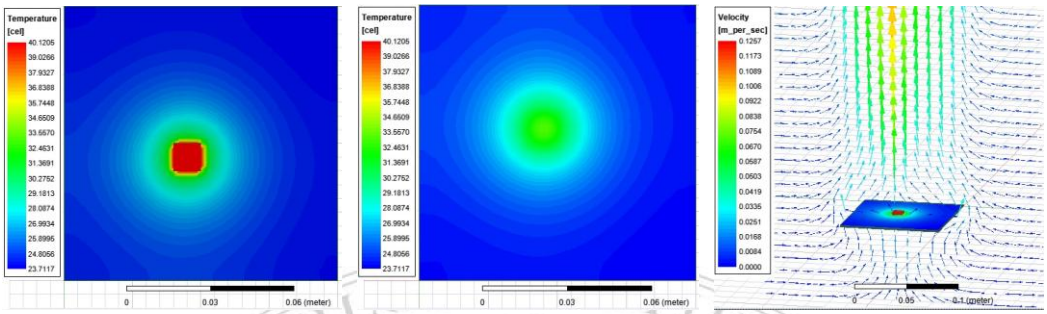


Fig. 2. STM32F405 Heat distribution on double sided PCB - Top view (left) and Bottom view (middle) and STM32F405 natural convection velocity vectors (right).

The simulation indicates a chip temperature around 40degC and an area of approximately 4 cm^2 on top and bottom of the PCB that had temperatures exceeding 32degC. As much as possible, in this area, no other high heat generating components will be placed.

DRV8301 is a complex circuit. Calculating the maximum power dissipation for a particular case would take a significant amount of effort. Estimating the power loss for a general case would be at this stage most beneficial. Further refinements could be made while analyzing a first prototype. The documentation provided by the producing company (TI) does not specify the amount of power that is lost in operation. To obtain an estimate, the focus will be on calculating the theoretical power loss of the major chip components: Inputs, output buffers, buck regulator, LDO's, Internal Logic. The data for the calculations will be supplied by the devices data sheet [2].

Inputs cumulate the signals for SPI, motor PWM and enable. The maximum current drawn, as indicated by term I_{IN_MAX} is 1mA. The internal resistance of the input circuitry is not provided, so an estimate of 5kOhm will be used. The power dissipated by one input is then 0.005W. Multiplied by the number of inputs: 4xSPI, 6xPWM, 2xEnable gives 0.06W.

Output buffers refer to MOSFET drivers and fault signals. Output MOSFET buffers can supply an RMS value of 30mA maximum. The ON resistance of the buffers is not provided in the data sheet, so it will be estimated to be around 100mOhm. The power dissipated by one output driver is 0.09mW. Total power dissipated by all 6 buffers is 0.54mW. The fault signals can sink a maximum of 7mA of current according to data sheet I_{SINK_MAX}. Provided that the R_{DS_ON} of the output transistors is ~100mOhm, a power of around 0.01mW is dissipated.

The buck regulator has at least one transistor that may dissipate significant amount of energy. Calculating power loss would involve calculating transistors

loss in different scenarios which is a tedious process. Since only a reasonable estimation is needed at this point and since the power loss is directly proportional to the regulator efficiency, a more simple solution could be found by estimating regulator efficiency and by relating it to output power generated by using the efficiency formula:

$$\eta = \frac{P_{OUT}}{P_D + P_{OUT}} \tag{1}$$

P_D is then:

$$P_D = P_{OUT}\left(\frac{1-\eta}{\eta}\right) \tag{2}$$

Efficiencies of buck regulators such as that found in DRV8301 usually fall between 90% and 95%. To have a safe margin of error, we will use an efficiency of 90%. The regulator will supply a maximum of 1A at 5V, so P_{OUT} lies around 5W. P_D is then

$$P_D = 5W * \left(\frac{1-0.90}{0.90}\right) = 0.56W$$

DRV8301 has two LDO's, A_{VDD} and D_{VDD}, whose power loss may be calculated by considering the output current and voltage drop:

$$P_D = I * (V_{IN} - V_{OUT}) \tag{3}$$

For A_{VDD}, output voltage is 6.5V, and the current provided is estimated at around 2mA.

$$A_{VDD} = (24V - 6.5V) * 0.002A = 0.035W$$

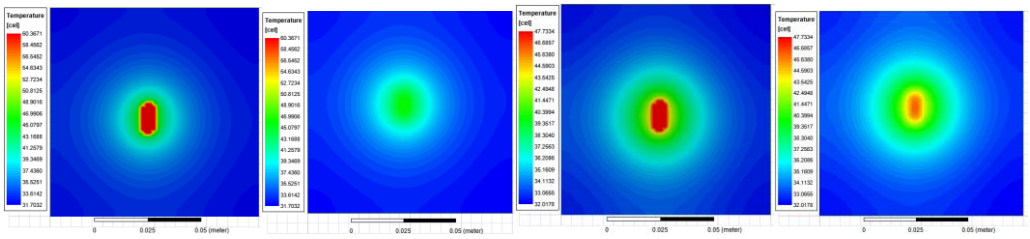
For D_{VDD}, output voltage is 3.3V, and the current provided is estimated at around 5mA.

$$D_{VDD} = (24V - 3.3V) * 0.005A = 0.15W$$

For DRV's internal logic we can only estimate a power consumption of 0.1W. Calculating the total power loss:

$$0.06W + 0.01W + 0.56W + 0.035W + 0.1W = 0.765W$$

DRV8301 has a maximum junction temperature T_J of 150degC. The most important thermal metric refers to junction to board thermal resistance $R_{\theta JB}$ which is 17.5 decC/W. This metric is important because the device is designed to be cooled by the PCB itself, using a thermal pad on the bottom for a better coupling to the board. Thermal vias and ground pours are needed on both layers. The following simulations indicate the temperatures to be expected in two cases: in the first scenario no thermal vias are used and in the second 9 vias with 0.4mm diameter and 15μm of copper plating are placed directly underneath the thermal pad. The ambient temperature is 20 degC in both cases.



a) b) c) d)

Fig. 3. DRV8301 Heat distribution on double sided PCB- No thermal vias – Top view (a) and Bottom view (b) DRV8301 Heat distribution on double sided PCB- With thermal vias - Top view (c) and Bottom view (d).

The impact of the thermal vias becomes immediately apparent when comparing - a) and b) with c) and d) in Fig. 3. The simulation indicates a 13degC difference between the two which corresponds to a 20% improvement. The simulation also indicates that at least 4 square centimeters should be present to provide minimal cooling.

AZ1117EH is a simple LDO regulator whose power dissipation can be easily obtained by using the voltage drop and maximum output current. The regulator is powering the microcontroller with a maximum of 240mA, encoders (2x12.5mA in case of magnetic encoders e.g. MagAlpha 702), analog circuitry (~5mA),

$$P_D = I * (V_{IN} - V_{OUT}) \tag{4}$$
$$P_D = 0.270A * (5V - 3.3V) = 0.459W$$

The maximum junction temperature T_J is 150degC according to data sheet [3]. The regulator comes in a SOT-223 package. For simulation purposes a simple rectangular block will be used. The copper coverage will be set to 70% to simulate the tracks in the regulator's circuitry. Ambient temperature is set to 20degC.

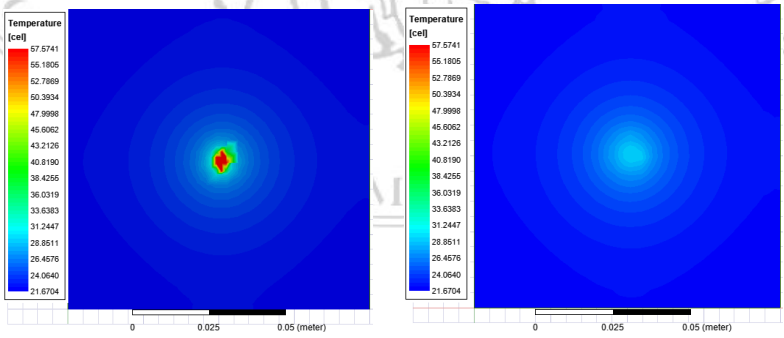


Fig. 4. AZ1117EZ Heat distribution on double sided PCB - Top view (left) and Bottom view (right).

The simulation indicates a maximum temperature on the board of around 58degC. A 1.5 square centimeters of PCB area provides adequate room for heat dissipation. The resistance from junction to board is not provided in the device's data sheet. However, based on information found in [4], this resistance for this type of package would be lower than 50degC/W, so we can expect a die temperature under 80degC which is acceptable.

Bulk capacitors

The life expectancy of an electrolytic capacitor is directly related to its internal temperature. Every 10degC increase in internal temperature halves the component lifetime. Capacitors are usually allowed to cool by natural convection, providing them with sufficient distance from nearby components. The capacitors used in this application are aluminum electrolytic capacitors. They were chosen because of their high volumetric efficiency (capacitance per unit volume) and the fact that they provide a high ripple current capability together with a high reliability and also because of their excellent price/performance ratio. The most common energy loss mechanisms inside these devices include dielectric losses, ferroelectric losses, dielectric conduction losses, interfacial polarization, partial discharge losses, ohmic resistance losses, sparking between conductors, electromechanical losses, and eddy current losses. Loses are greatly affected by frequency and ambient temperature. The data sheet of the component gives the relevant operating parameters at 120Hz and 20degC. These conditions are acceptable for this application, although the frequency might be somewhat higher, but nevertheless will produce an estimate close enough to reality.

According to [5], he dielectric losses ($P_{dielectric}$) are as follows:

$$P_{dielectric} = \hat{u}_{ac}^2 * \pi * f_0 * C * tan\,\delta_0 \quad (5)$$

$\hat{u}_{ac}$ - peak value of symmetrical AC ripple voltage applied to capacitor [V]
f_0 - fundamental frequency Hz of the ripple voltage
C - capacitance
tan δ_0 - dissipation factor of capacitor dielectric

$$P_{dielectric} = 2^2V * \pi * 120Hz * 470 * 10^{-6}F * 0.12 = 0.085W$$

The resistive loses are according to [6]:

$$P_{resistive} = I_{rms}^2 * ESR \quad (6)$$

I_{rms} - root mean square value of capacitor current;
ESR - equivalent series resistance Ω.

Equivalent Series Resistance (ESR) is the sum of the ohmic losses of the dielectric, materials and connections used in the construction of the capacitor and can be easily determined on the base of $tan\ \delta_0$. The tangent is found on a regular basis on capacitors data sheet. As this value is frequency dependent, it is provided alongside the corresponding frequency. For aluminum electrolytic capacitors the frequency at which the measurement is provided is 120Hz. The ripple current in this application might be higher, but the estimate will still be relevant.

$$ESR = tan\ \delta_0 * X_C = \frac{tan\ \delta_0}{2 * \pi * f_0 * C} \tag{7}$$

$$ESR = \frac{0.12}{2 * 3.1415 * 120Hz * 470 * 10^{-6}F} = 0.338ohm$$

The RMS value of the ripple current is not as easy to determine. It depends on the inductance (L) and resistance (R) of the motor windings, the time constant of the winding ($\tau = L/R$) the state the motor is in, voltage applied (V_{DCBUS}), PWM period (T), back EMF (E) and duty-cycle (D) (Fig. 5).

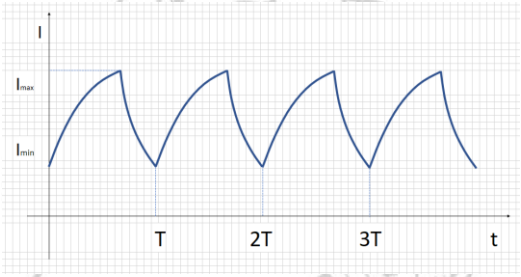


Fig. 5. Ripple current during PWM switching.

The ripple current has two stages. A stage in which it rises, when the transistor bridge turns current ON into the winding, which we will note as I_{ON}, and a stage in which it falls, when the bridge transistors turn off the current supply in the winding, leaving the energy accumulated in the windings inductance flow in the bridge diodes, which we will note as I_{OFF}. According to [7], [12], the equations describing the rise and fall of the current in the winding are as follows:

$$I_{ON}(t) = I_{min}e^{\frac{-t}{\tau}} + \frac{V_{DCBUS} - E}{R}(1 - e^{\frac{-t}{\tau}}) \tag{8}$$

$$I_{OFF}(t) = I_{max}e^{\frac{-(t-DT)}{\tau}} - \frac{E}{R}(1 - e^{\frac{-(t-DT)}{\tau}}) \tag{9}$$

Choosing the I_{min} and I_{max} on the I_{ON} and I_{OFF} curves respectively we get:

$$I_{ON}(DT) = I_{max} \quad and \quad I_{OFF}(T) = I_{min}$$

$$I_{min} = -\frac{E}{R} + \frac{V_{DCBUS}}{R} * \left(\frac{e^{\frac{(1-D)T}{\tau}} - e^{\frac{T}{\tau}}}{1 - e^{-\frac{T}{\tau}}}\right)$$

Solving at these points: (10)

$$I_{max} = -\frac{E}{R} + \frac{V_{DCBUS}}{R} * \left(\frac{1 - e^{-\frac{DT}{\tau}}}{1 - e^{-\frac{T}{\tau}}}\right)$$

we get the ripple current

$$I_{max} - I_{min} = \frac{V_{DCBUS}}{R} * \frac{(1 - e^{-\frac{T}{2\tau}})^2}{1 - e^{-\frac{T}{\tau}}}$$

The ripple current is at maximum when the duty-cycle is 50% and is zero at 0% and 100%. For the 50% duty cycle condition, the worst case is when the full V_{DCBUS} is applied, that is when back EMF is zero and thus the motor is stationary (start-up or stall condition). This application is using a V_{DCBUS} of 20V, motors with winding resistance of around 150mOhm, a minimum inductance of 25uH and a switching frequency of 24kHz. Using these conditions and assumptions we are provided with the values shown below:

$$V_{DCBUS} = 20V; \quad R = 150 * 10^{-3} Ohm; \quad \tau = 0.167 * 10^{-3} s; \quad T = 4.2 * 10^{-5} Hz$$

$$I_{max} - I_{min} = \frac{V_{DCBUS}}{R} * \frac{\left(1 - e^{-\frac{T}{2\tau}}\right)^2}{1 - e^{-\frac{T}{\tau}}} \cong 8.5\ A$$

If we approximate the ripple current function with a simple triangle function, we can calculate the RMS value in a more convenient way:

$$I_{rms} = \frac{I_{ripple}}{\sqrt{3}} \cong 4.8A$$

The I_{rms} value of the ripple current is distributed between 2 types of capacitors [11]. One is a MLCC 10uF and the other type is an aluminum electrolytic with a capacitance of 470uF. The smaller capacitor has a low ESR, 20mOhm as indicated by the data sheet, and is able to surge currents very fast, while the bigger one, with its 338mOhm as calculated earlier, will kick in later in the cycle. How much of the ripple current would be supplied by the smaller capacitor versus the largen one, can be calculated based on energy flowing in the motor winding. At 50% duty cycle and with a stalled motor, the I_{rms} value has its maximum. To visualize the currents from the two capacitors, a SPICE simulation was conducted using ANSYS Nexxim. The circuit has a simulated ideal DC power supply to which its impedance was added in form of lumped R, L and C, plus the estimated wire resistance. The two capacitors are formed by using ideal capacitor in series with a resistor to simulate its ESR. The chopping circuit was build based on a pulse generator, a half diode bridge and a voltage-controlled switch (Fig. 6).

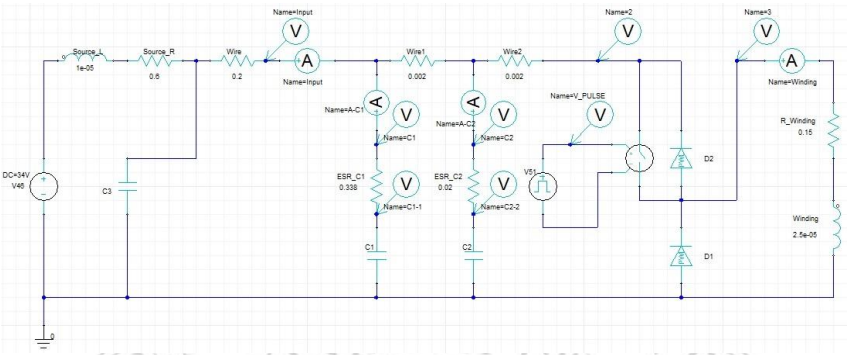


Fig. 6. Capacitor simulation circuit in Nexxim.

The current in the bulk capacitors receives the main focus, along with the total current in the winding. The currents are graphically shown in the Fig. 7.

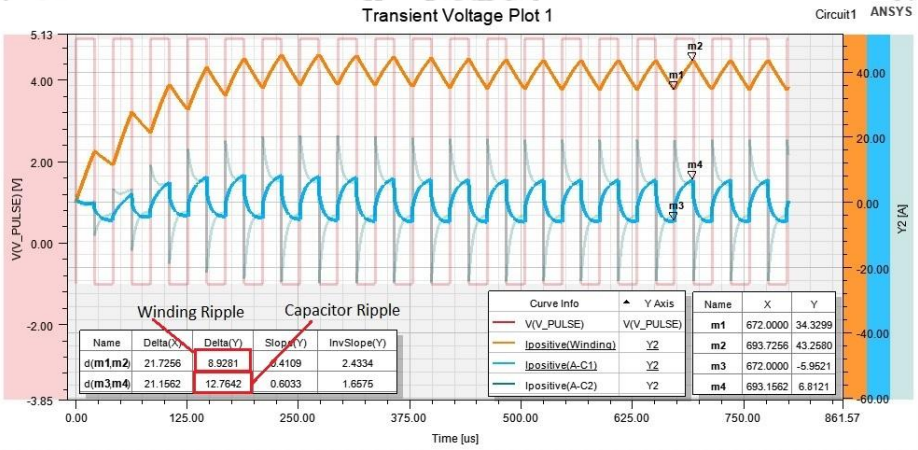


Fig. 7. Circuit currents: Winding current in orange, 470µF capacitor current in blue, 10µF capacitor current in shaded blue and chopping voltage in shaded red.

The simulation indicates a ripple current in the motor winding of 8.9281A, on a par with the theoretical calculated value. However, the ripple current in the capacitor is larger, having a value of 12.76A as indicated by the simulation. This is because the larger capacitor starts providing a large current later in the cycle, as the first part is covered by the smaller and faster acting capacitor. As seen in the Fig. 8, the RMS value of 4.66A is still as anticipated, a little bit lower than the RMS value of the winding current which lies around 4.8A. The difference is of course largely covered by the smaller capacitor and possibly a small part directly by the power supply.

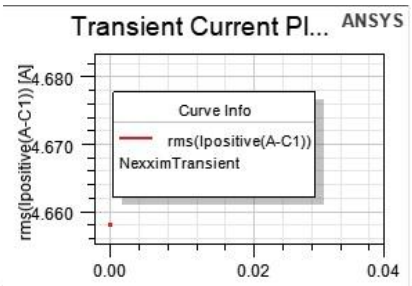


Fig. 8. 470μF capacitor RMS value.

The RMS value of 4.6A is much too large for the 470μF capacitor, which according to its data sheet can only withstand 1.1 A (Fig. 8). Therefore, we need to consider the situation in a more practical way. A maximum winding current of 43A was obtained using simulation, which is much larger than the maximum 30A allowed by the application. It is clear that a duty cycle of 50% for the given motor will never be possible. The simulation was rerun with a duty cycle that will produce a maximum of 30A. The results are indicated in the Fig. 9. The duty cycle is reduced to 23% from 50% and the winding current reduces from 43A to 30A.

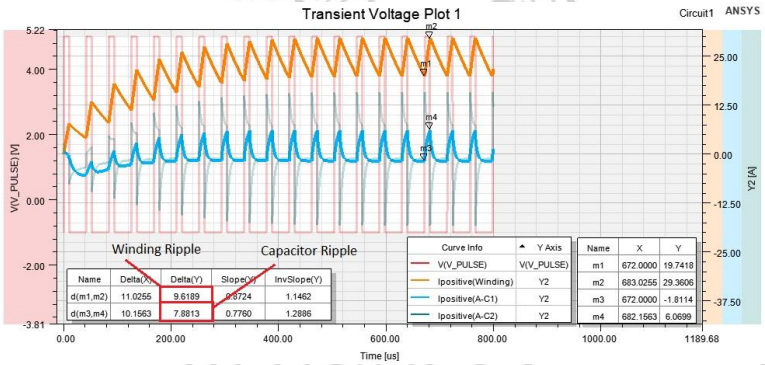


Fig. 9. Simulation rerun with a duty cycle of 23% and a maximum winding current of 30A.

Fig. 10 shows the newly calculated RMS value after simulation rerun. A value of 2.6A is indicated, which is 40% lower than the previous one.

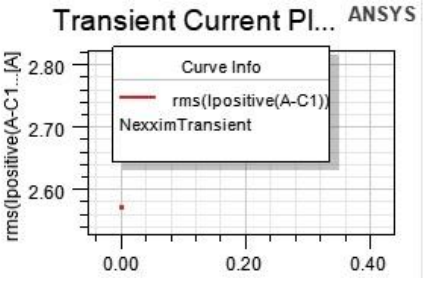


Fig.10. RMS value of the 470μF capacitor after simulation rerun.

The RMS value of the ripple current across the capacitor is still significantly larger than the maximum allowed by his construction. However, this value is still largely theoretical since it is only produced when the motor is stalled while producing maximum torque. It will only be produced in one of the three windings at a certain moment in time and since it is a stall condition, it will produce a servo "following error" in maximum a second, which in turn will cut the motor power. We will assume a more feasible maximum of 2A of ripple current RMS. We will need to spread this ripple across a minimum of two capacitors in parallel. We will assume a balanced load on the capacitors, so we will calculate the power loss on one capacitor based on a 1A current.

$$P_{resistive} = I_{rms}^2 * ESR = 1^2 A * 0.338 ohm \cong 0.4W$$

To the resistive power loss, the dielectric loss is added:

$$P_{tot} = 0.085W + 0.4W = 0.485W$$

We will use the value of 0.5W of dissipated power in one capacitor, which seems like a reasonable value. For simulation purposes a simple cylinder block will be used. The copper coverage on the PCB will be set to 70% to simulate the tracks in the regulator's circuitry. Ambient temperature is set to 20degC.

Current sense resistors and MOSFETs

Current sense resistors have a value of 2mOhm and will have a peak current of maximum 30A flowing through them. We can estimate a RMS value of 22A giving the fact that the current wave form is a sinusoid composed out of a 24kHz base frequency and its 3rd harmonic at 72kHz. The power dissipated through heat is then 0.96W. These devices are placed in the close vicinity of the power transistors and therefore will be simulated together with them.

The power loss in a MOSFET transistor is governed mainly by its internal drain to source ON resistance, its switching characteristic and its integrated flywheel diode loses.

$$P_D = P_{RDS} + P_{switch} + P_{diode} \quad (11)$$

The power dissipated during the ON states is relatively simple to estimate:

$$P_{RDS} = R_{DS(ON)} * {I_{rms}}^2 \quad (12)$$

The $R_{DS(ON)}$ is provided by the transistors data sheet [8], including the derating induced by temperature. At 25degC the transistor has a resistance of 1.7mOhm. At 150degC junction temperature, the resistance derates with approximately 1.65. We will use the worst-case scenario and we will calculate the power loss at the highest junction temperature:

$$R_{DS(ON)} = 1.7 mohm * 1.65 = 2.8 mohm$$

As stated earlier, the I_{rms} is 22A, so the power loss is then:

$$P_{RDS} = (22A)^2 * 2.8 mohm = 1.36W$$

The transistor's switching loss is difficult to calculate as it depends on many hard-to-quantify and typically unspecified factors that contribute to the turn-on and turn-off events. To get an insight and to be able to evaluate the process, we can estimate the power loss taking into account the major elements that come into play: the voltage across the motor windings V_M, the winding RMS current I_{rms}, the Miller charge Q_{GD} (also referred to as reverse transfer charge), driver source/sink current capability I_{source} /I_{sink} and switch frequency f_{switch}. The driver has the ability to source and sink three different current levels. For this estimation the middle value was chosen: 0.7A.

According to [9], the switching losses are:

$$P_{switch} = P_{rise} + P_{fall}$$

$$P_{rise} = \frac{V_M * I_{rms} * f_{switch} * t_{rise}}{2} \qquad (13)$$

$$P_{fall} = \frac{V_M * I_{rms} * f_{switch} * t_{fall}}{2}$$

The calculation of t_{rise} and t_{fall} is based on equations found in [10]:

$$t_{rise} = \frac{Q_{GD}}{I_{source}} = \frac{4.7nC}{0.7A} = 6.7ns$$

$$t_{fall} = \frac{Q_{GD}}{I_{sink}} = \frac{4.7nC}{0.7A} = 6.7ns \qquad (14)$$

$$P_{rise} = \frac{20V * 22A * 24000Hz * 6.7 * 10^{-9}s}{2} = 0.035W$$

$$P_{fall} = \frac{20V * 22A * 24000Hz * 6.7 * 10^{-9}s}{2} = 0.035W$$

The power loss inside the flywheel diode is:

$$P_{diode} = R_{diode} * {I_{rms}}^2 * duty \qquad (15)$$

At 150degC, the diode resistance is, according to [8], lower than 0.0075Ohm. The diode will flywheel current for a very short amount of time determined by the dead time setting of the bridge driver. We consider it to be around 1% duty.

$$P_{diode} = 7.5mohm * (22A)^2 * 0.01 = 0.036W \qquad (16)$$

The total power dissipated inside the transistor chip:

$$P_D = P_{RDS} + P_{switch} + P_{diode} = 1.36W + 0.035W + 0.035W + 0.036W \cong 1.5W \qquad (17)$$

Fig. 11 shows the heat distribution in case of a MOSFET and its corresponding sense resistor. The PCB is 100x100mm and has 70% copper to simulate traces, the ambient temperature is 20degC. Thermal vias are located around the devices

on an area of 2 cm^2. The via density is 1 per 4 mm^2. The maximum junction temperature of the MOSFET, T_J is 150degC according to data sheet [8]. The transistor comes in a SO-8FL package. For simulation purposes a simple rectangular block will be used.

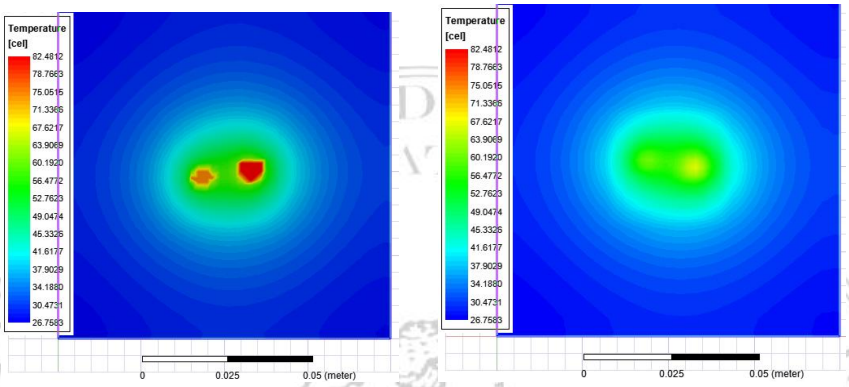


Fig.11. MOSFET(right in each picture) and sense resistor(left in each picture) - Heat distribution on double sided PCB with 1 thermal via per 4mm^2- Top view (left) and Bottom view (right).

MOSFETs are the main heat generators, so finding the minimal copper area that will permit a safe operation is of main importance. We will try to keep the junction temperature of the device below 130degC. Considering a thermal resistance of 30 degC/W between PCB and junction, we need to aim for a maximum of around 100degC peak temperature on the PCB surface.

Fig. 12 shows the heat distribution and the maximum temperature when the two devices are placed on a 30x30mm PCB with 1 thermal via per each 4mm squared and with 90% copper area density on both top and bottom layer. The maximum temperature of 105degC is reached which provides an acceptable solution.

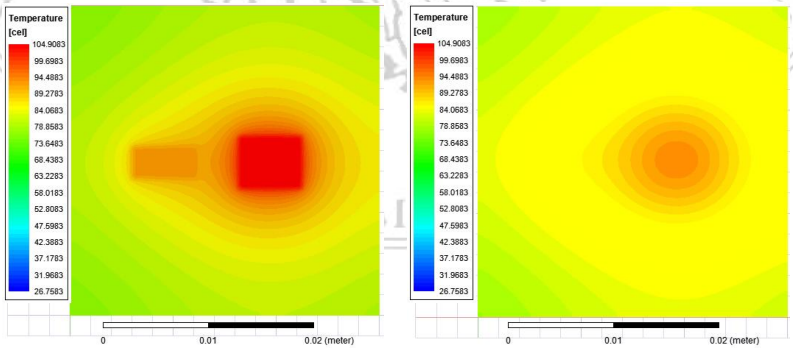


Fig. 12. MOSFET(right in each picture) and sense resistor(left in each picture) - Heat distribution on double sided PCB 30x30mm with 1 thermal via per 4mm^2- Top view (left) and Bottom view (right).

3. Conclusions

Each device has a certain amount of PCB space that it requires to receive adequate cooling. A few arrangements based on trial and error were tried. The best solution was found to be the one that had the hottest components placed on the outer side of the board, while keeping the cooler ones in the middle of the board. Since the MOSFETS are the most problematic from the heat generation perspective, and since they require the most space, they were arranged on the margins. The PCB design would have ideally used no more then 100mmx 100mm of space. It turns out that that space is not enough. In theory, 120mmx120mm is the smallest space required to keep all components at their highest safe temperature. Fig. 13 shows an unexpected result. The transistors show a board temperature of 124 degC, much higher than expected. It is clear, that when all components are placed together, the cumulated effect is much bigger than anticipated.

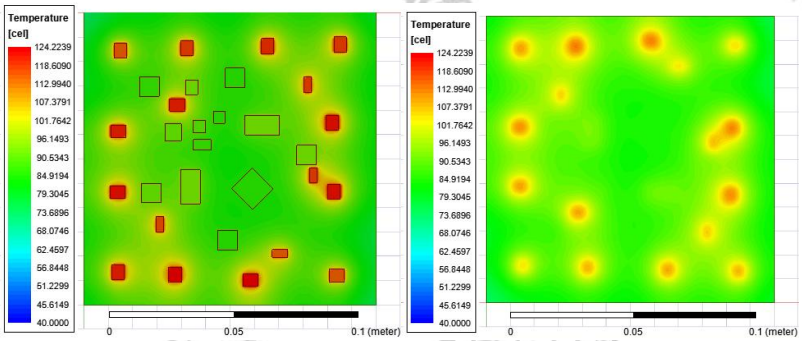


Fig. 13. All components placed on double sided PCB with 1 thermal via per 4mm2- Top view (left) and Bottom view (right).

Under these circumstances, the solution to the aforementioned problem could be an enlargement of the board, a forced air flow over the board, the mounting of heatsinks over the transistors or a combination of the previous. Fig. 14 and Fig. 15 show the simulation results in case an air flow of 0.25 m/s blown over the board. The results show significant improvement, as the temperature drops by more than 25 degC and stabilizes below the maximum allowed.

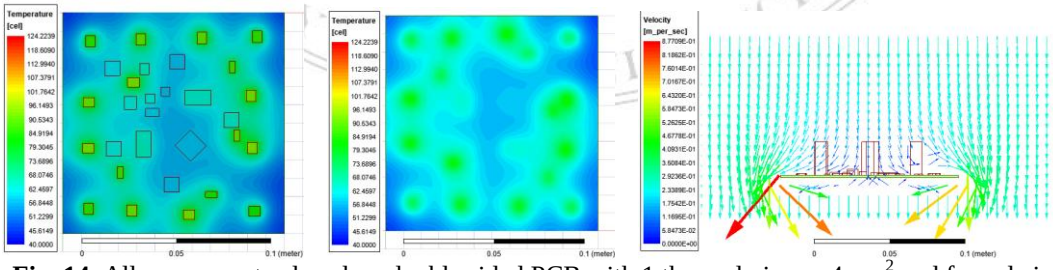


Fig. 14. All components placed on double sided PCB with 1 thermal via per 4mm^2 and forced air flow of 0.25m/s perpendicular to the top of the board- Top view (left) and Bottom view (middle); Flow vectors (right).

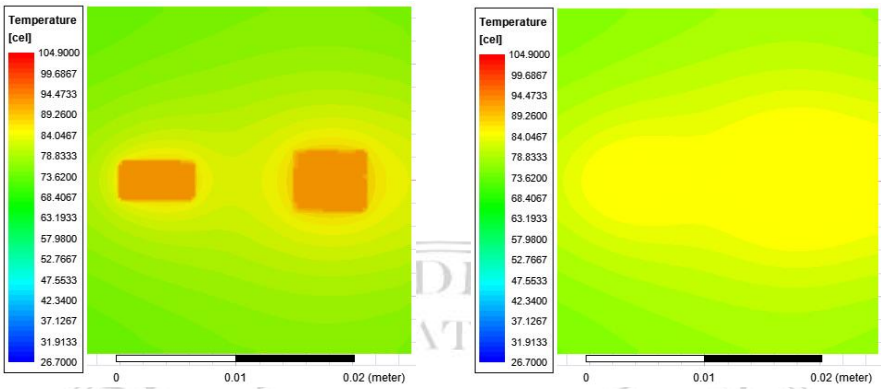


Fig. 15. MOSFET(right in each picture) and sense resistor(left in each picture) - Heat distribution on double sided PCB 30x30mm with 1 thermal via per 4mm2 with heat sink mounted on transistor- Top view (left) and Bottom view (right).

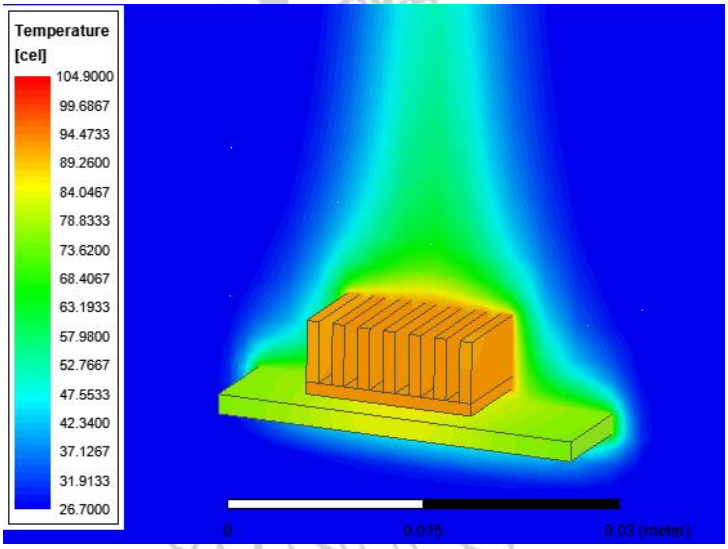


Fig. 16. Heat distribution on transistor heat sink.

Mounting heatsinks on transistors also brings the board to a safe operation region as far as temperatures are concerned.

Final simulations are made with a single transistor with heat sink attached and current sense resistor on a 3cmx3cm PCB with 90% coverage of 1 oz. copper cladding on each side and with 1 thermal via at each 4 mm^2.

The heat sink has a base of 14mmx14mm, a height of 6mm and has 7 fins (Fig. 16). The ambient temperature was set to 20 degC.

R E F E R E N C E S

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