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A STRUCTURED, TOP-DOWN DESIGN METHODOLOGY FOR THE DESIGN OF THE LOW FREQUENCY PART OF MULTI-STANDARD RADIO RECEIVERS FRONT-ENDS

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Radio receptoarele multi-standard (SDRXX) moderne reprezintă un bloc funcţional cheie din componenţa circuitelor integrate utilizate în communicaţiile radio. Lucrarea prezintă o metodă nouă de proiectare a părţii de joasă frecvenţă a unui radio receptor multi-standard cu conversie directă de frecvenţă bazat pe condiţionarea analogică a semnalului. Metoda se bazează pe analiza structurată la nivel de sistem urmărind identificarea constrângerilor cheie – corespunzătoare aplicaţiilor radio considerate, asupra arhitecturii circuitelor. Concluzia care rezultă în urma acestei analize este că pentru implementarea receptoarelor multi-standard moderne trebuie folosită o arhitectură modulară, bazată, în cazul de faţă, pe amplificatoare cu reacţie negativă de joasă putere, care facilitează transferul circuitului într-un proces CMOS cu detaliu critic mai mic. În final se prezintă analiza blocului funcţional cheie din perspectiva unei utilizări într-un mediu multi-standard şi sunt prezentate motivele care au stat la baza alegerii soluţiei de circuit care optimizează atât consumul de putere cât şi liniaritatea circuitului.

Today's Software Defined Radio Receivers front-ends (SDRRX) represent a key building block in communication chips. This paper presents a structured, top-down, system level to circuit level design methodology used in building the modern direct conversion SDRRXs low frequency (LF) part. This methodology is aimed at first to identify the key system level constraints and, thus, choose the optimal architecture for the SDRRX low frequency (LF) part. Subsequently, once the SDRRX LF part key requirements have been identified, the design methodology focuses on the optimal features of the circuit level implementation given the multi-standard application. The paper details why a modular architecture based on low power fully differential amplifiers is best in managing the receiver noise and linearity performance as well as alleviating technology issues associated with deep sub-micron CMOS processes and thus enabling the design porting.

Keywords. Software Defined Radio Receiver Front-End, System Level Analysis.

1. Introduction

Today's Software Defined Radio Receivers front-ends (SDRRX) represent a key building block in communication chips.

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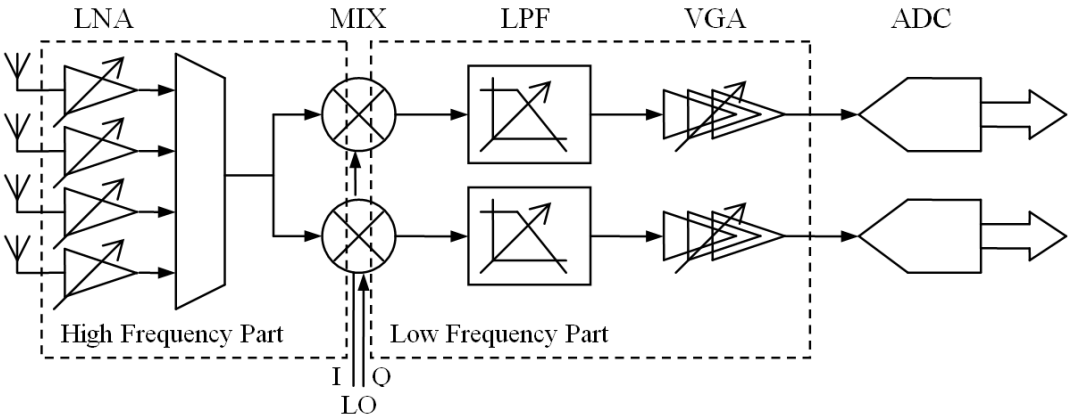

Fig. 1 – Generic SDRRX block diagram [1].

This paper presents a structured, top-down, system level to circuit level design methodology used in building the modern direct conversion SDRRXs low frequency (LF) part.

The block diagram of a direct conversion SDRRX that uses analog channel selection is shown in Figure 1 [1]. This receiver front-end topology is well known and its usage for multi-standard radio applications is natural [2]. The authors have been actively involved in the past years in analyzing the architectures used in designing such as mixer-based direct conversion multi-standard radio receivers [1, 3, 4] and in the study of the key trade-offs that shape their design process [5, 6]. The receiver is split in two parts: a high frequency (HF) part formed by the LNAs and the downconversion mixer and a low frequency (LF) part made out of the mixer's transimpedance amplifier (TIA), the low pass filter (LPF) and the variable gain amplifier (VGA).

The main focus of the paper is to disclose the novel system level driven design methodology for the LF part of the SDRRX. The baseband circuit design for multi standard radio applications has been addressed in several publications so far (e. g. [7]). But, in todays design environment the key SDRRX features are stemming from the system level analysis. In the recent works, the authors emphasize the importance of the system level analysis in building power and area efficient receiver designs for multi-standard radio receivers [8, 9].

Hence, Section 2 introduces the key system level aspects that shape the SDRRX LF part design and presents the modular architecture based on low power, low noise and highly linear fully differential feedback amplifiers multi-standard. Section 3 explains the optimal design choice for baseband amplifier design considering the multi-standard design constraints. Finally, Section 4 concludes the paper.

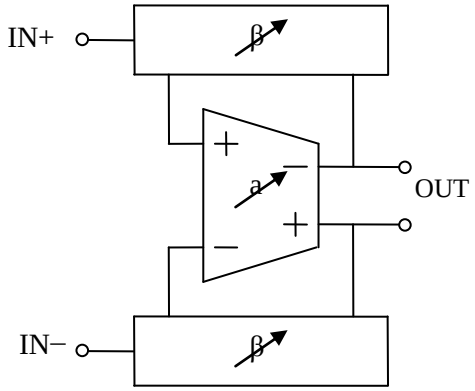

Fig. 2 – SDRRX LF part building brick.

2. Defining the Modular Architecture as the Optimal Implementation for the SDRRX LF Part

The multi-standard environment is characterized by several key parameters that have different values for every wireless standard or even within the same standard. These parameters are the RF frequency plan, the signal bandwidth and the minimum signal-to-noise ratio that enables a proper demodulation. The authors have highlighted the values of these parameters for the present day key wireless standards in [10].

Hence, the designer must be enabled to handle efficiently the noise and linearity performance of the system regardless of the values of the various parameters listed before and of the CMOS process feature that is being used.

For the SDRRX LF part design its noise performance is less critical due to the RF stages gain, while its operation must be very linear, considering the lack of significant filtering on the RF path. Given the rather low baseband signal frequency for the wireless standards (i. e., up to a few tens of MHz), the use of negative feedback in the analog signal conditioning path of the SDRRX LF part blocks is the optimal solution to control the system linearity. Thus, it becomes natural for the SDRRX LF chain blocks to be implemented with low power fully differential feedback amplifiers (FDFAs), redrawn in Figure 2. As in-depth analyzed in [1], the FDFAs highly linear operation is due to their high loop gain at the maximum frequency of interest and to the linear elements in the feedback network (i. e., metal-insulator-metal capacitors and poly-Si resistors). Given the variable baseband channel bandwidth, specific to the multi-standard implementation, the feed-back network RC ladder is to be made programmable. Some programmability is also required in the opamp, as it will be detailed in Section 4.

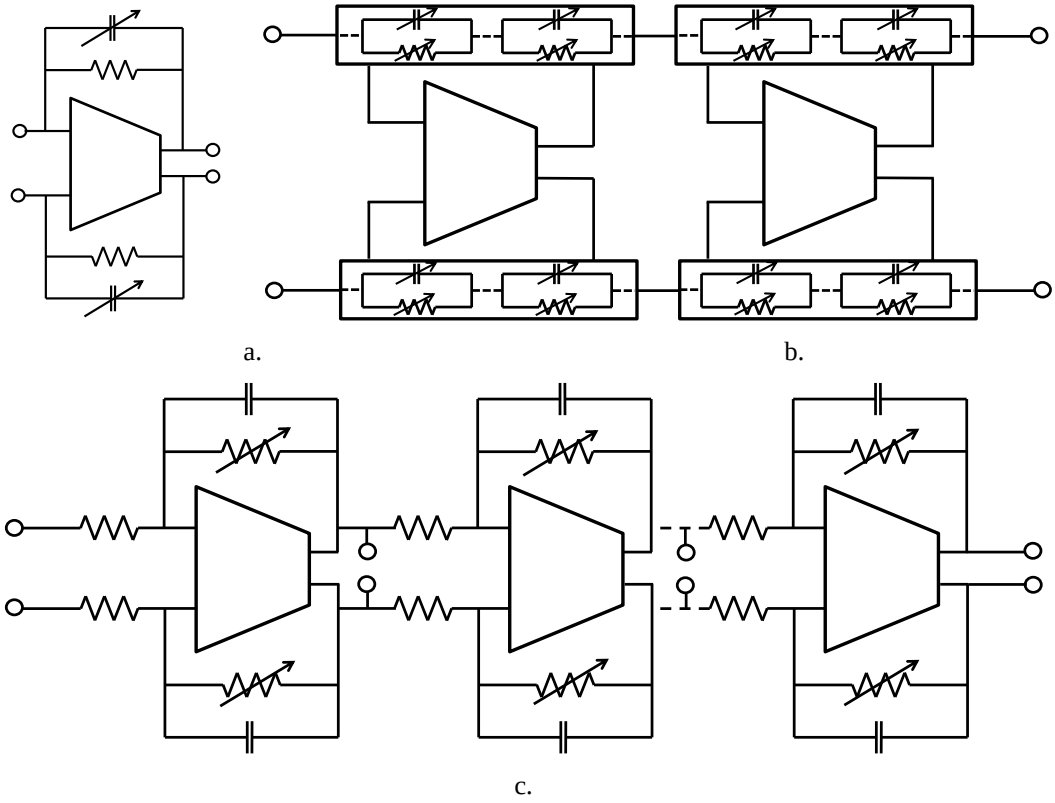

Fig. 3 – The modular architecture of the SDRRX LF blocks
a. mixer TIA stage; b. the LPF and c. the VGA.

The FDFA is assumed to have a voltage feedback at the input and a current feedback at the output of the base amplifier. Thus, the system acts as a voltage amplifier. Managing voltages represents the natural solution in the analog conditioning of the downconverted RF signal in a CMOS process, which benefits from the capacitive input impedance of the MOS device.

Moreover if used efficiently this approach enables the design porting to lower feature size CMOS processes with minimal design effort and with best results. The negative feedback will inherently alleviate specific issues of a deep-submicron CMOS implementation (e. g., leakage).

Thus, all the SDRRX LF blocks (i. e., the TIA, the LPF and the VGA) will be implemented by using a sequence of modules based on the FDFA of Figure 2, as it is shown in the example of Figure 3.

First the mixer transimpedance amplifier will be based on one single FDFA cell embedding a simple, one pole, RC feedback network. Thus, the mixer stage has also a first order low pass filter characteristic that will reduce the level of near-by blockers.

Second, the LPF order, and thus the number of FDFA cells that will be used in building it, is given by the key trade-off shaping the SDRRX LF part design. In [5] the authors have analyzed in-depth this trade-off between the LPF order and the ADC specifications of resolution and speed. For the most popular wireless standards an analog LPF order of 4 was found as the optimal choice; hence the representation of two bi-quad cells in the example of Figure 3.b, each made of one FDFA circuit with RC feedback. Nevertheless, considering the fast rate at which the ADC power efficiency improves the analog LPF order, and thus the RX area, the LPF can be further reduced.

Finally, the VGA generic block diagram is depicted in Figure 3.c. The optimal number of stages is found from the trade-off between the circuit linearity and its power consumption. In [11] the authors have analyzed the optimal number of stages for a VGA build for wireless applications and found that 7 stages represents the optimal choice for a dynamic range of 84 dB. Each stage is made out of a FDFA with a feedback network made out of programmable feedback resistors to achieve the variable gain in parallel with an optional feedback capacitor that limits the noise bandwidth.

3. Baseband Amplifier Power Optimisation Considering the Multi-standard Design Constraints

Once the SDRRX LF blocks topology has been defined, the designer focus shifts towards identifying the constraints of the multi-standard environment on the key active component that is the baseband amplifier.

A multi-standard environment assumes multiple bandwidths for the baseband channel. Lately, variable signal bandwidths are foreseen even within the same wireless standards.

Thus, the SDDRX LF part bandwidth needs to be made programmable by implementing the FDFA feedback network with programmable arrays of resistors and capacitors. A one stage design for the base amplifier would be sensitive to changes in its feedback network, since its load is actually changing depending on the wanted bandwidth value. Thus the optimal choice for the opamp is to be implemented by two stages. The opamp output stage acts as a buffer, and thus reduce the loading effect on its intrinsic parameters, mainly on the opamp gain-bandwidth product (GBW).

A true re-configurable receiver must optimally trade-off its power consumption with the baseband signal bandwidth. The major constraints on the FDFA current consumption are set by four factors: Noise, Linearity, Stability and Current driving capability. Further on we will address the four factors from the perspective of a flexible baseband bandwidth.

Table 1

The Major Constraints on the FDFA Power Consumption

Parameter	Impact on the opamp power consumption
Noise	Sets a first lower limit for the opamp first stage current, as the noise performance is inverse proportional with the first stage transconductance, g_{mI}
Linearity	Sets another lower limit for the opamp first stage current, as the FDFA linearity performance is proportional with BW/GBW and GBW is set by g_{mI}.
Stability	Sets a first lower limit for the opamp second stage current, as the phase margin is proportional with the second stage transconductance, g_{mII}
Current drive	Sets another lower limit for the opamp second stage current required to prevent slewing

First of all, for all the envisaged standards, the receiver foresees a 3 dB minimum NF and, thus, a constant noise spectral density for the baseband chain blocks [12]. This first constraint blocks the current through the FDFA base amplifier input stage and sets the feed-back network resistors value.

Secondly, the FDFA linearity performance is proportional with BW/GBW, the ratio between the maximum frequency of interest (BW) and the opamp GBW [1, 4]. Hence, for the standards with smaller BW, the opamp GBW can be also lowered accordingly.

Thirdly, the FDFA opamp stability requirement (i. e., a phase margin larger than 60°) are met with enough output current in the final opamp stage. When the required BW is smaller, the feedback network capacitance will be increased accordingly. This capacitance (in the order of a couple pF) is the dominant part of the opamp load capacitance. This constraint blocks the output stage quiescent current.

Finally, the output stage current drive capability should be the same with respect to the variable signal bandwidth. Since the output stage current drive capability is linked to the DC quiescent current, it naturally results the optimal choice for a power efficient design is a class AB output stage.

Table 1 summarizes all the impact of all these constraints on the FA base amplifier design.

4. Conclusions

This paper presented the structured, top-down, system level to circuit level design methodology used in building the modern direct conversion SDRRXs LF part. After the key system level constraints are identified, becomes clear that the

circuit must handle efficiently the noise and linearity performance. Thus the optimal SDRRX LF part architecture consists of a modular implementation based on low power FDFAs embedding a linear feedback network based on poly-Si resistors and on metal-insulator-metal capacitors. Given the rather low frequency of the baseband signal bandwidth, the negative feedback provides the most power efficient method to control the system's linearity and noise performance. Also, it is the best option to alleviate the side effects of deep sub-micron CMOS processes (e. g., leakage). Finally, and most importantly in today's design environment, the usage of a modular concept facilitates design porting to newer lower feature size of the CMOS technological node.

Thus, from the circuit design point of view, the designer main focus is the power optimization of the FDFA base amplifier. Since the multi-standard environment is characterized by multiple signal bandwidths, the FDFAs feedback networks will contain programmable arrays of resistor and capacitor elements. Thus, a two stage opamp design alleviates the loading effect of the programmable RC array on its intrinsic parameters, mainly on its gain-bandwidth product (GBW). And a class-AB output stage is the optimal choice for improving the opamp's power efficiency.

A C K N O W L E D G M E N T

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