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MAKING HOMODYNE RECEIVERS READY FOR MONOLITHIC INTEGRATION IN MULTI-STANDARD WIRELESS TRANSCEIVERS

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Abstract. *This paper examines the main issues of homodyne receiver architecture with respect to its monolithic integration in a multi-standard wireless transceiver. The paper's main goal is to find out the architectural changes required to reduce the sensitivity of the zero-IF receiver topology to DC offsets and self mixing process. Based on the presented analysis, the receiver must foresee a DC offset calibration loop and high frequency wide-band frequency dividers in order to facilitate the monolithic integration of the direct conversion architecture, the most suited architecture for a re-configurable multi-standard radio receiver. The paper emphasizes the general character of the proposed implementation, as it fits best a true re-configurable multi-standard implementation.*

Keywords: Software Defined Radio, Direct Conversion Receiver, Receiver Sensitivity, DC Offset Compensation, Dynamic Offset

1. Introduction

The homodyne quadrature down-converter architecture provides the optimum solution for the implementation of Re-Configurable Multi-Standard Radio Receivers, [1]. First of all, in direct conversion receivers the useful signal is its own image: therefore, there is no image to reject and hence no need for an additional image rejection filter. Furthermore, all baseband processing, like analogue filtering, baseband amplification, analog-to-digital conversion and the digital demodulation, take place at the lowest possible frequency. These features make the homodyne receiver an ideal candidate for monolithic integration.

The homodyne receiver block schematic is presented in Fig. 1. The received RF signal is amplified by the low noise amplifier (LNA), then downconverted directly to baseband by mixing with a local oscillator (LO) signal of the same frequency. After the mixer, the baseband signal is filtered by the anti-alias Low Pass Filter (LPF). Subsequently, the Variable Gain Amplifier (VGA) boosts the signal such as the Analog-to-Digital Converter (ADC) to be optimally loaded.

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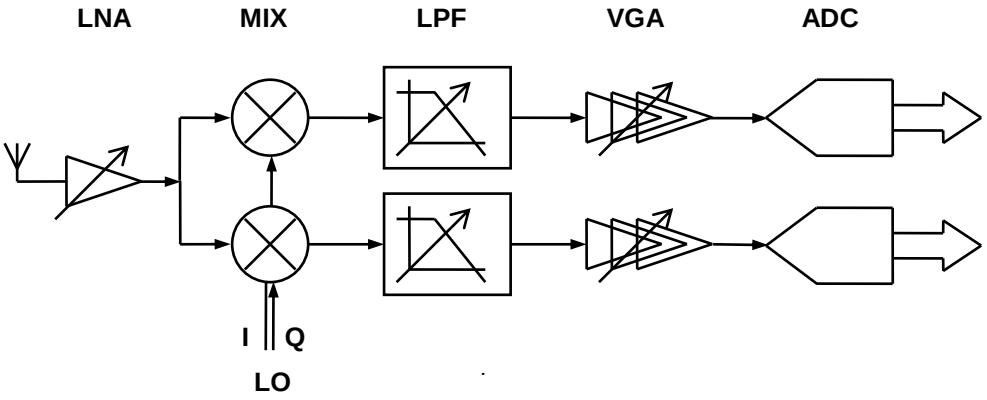

Fig. 1. Quadrature direct conversion receiver block schematic.

However, although direct conversion receivers monolithic integration seems straight forward there are several drawbacks to this approach. Firstly homodyne architecture is extremely sensitive to static DC offsets and 1/*f* noise. As the signal is directly converted to baseband, receiver noise figure is affected by 1/*f* noise.

Generally the mixer output is DC coupled to the LPF, since a major part of the received signal baseband spectral energy is located at low frequency (i. e. the GSM standard).

Regular AC coupling will not solve the issue, as receiver settling will be severely affected by a low cut−off frequency in the order of a few hundred Hz.

Given the large VGA gain, usually larger than 60 dB, [2], the receiver output risks of being overloaded even for small values of the DC offset, in the order of a few hundreds μV.

The second major issue of the Fig. 1 receiver architecture is even order distortions generate a signal dependent DC offset.

As the received input power can change dynamically, since other transmitters may start to transmit, a dynamic offset component is generated due to the receiver second order non-linearity.

Also, the self mixing process, determined by the LO mixing with the LO signal leaking from the VCO to the receiver input, can generate a large DC offset overloading the receiver output.

The paper's main goal is to determine the architectural changes in the Fig. 1 receiver, required to compensate the above mentioned issues and to facilitate its monolithic integration into a multi-standard wireless transceiver. The main target is to build a receiver architecture framework compatible with the most popular wireless standards using a frequency plan up to 3 GHz, as noted in Table 1.

Table 1

Frequency Plan and Maximum Baseband Channel Bandwidth for the Major Wireless Standards

Wireless Standard	Frequency Plan [MHz]		Maximum Baseband Bandwidth [MHz]
	Uplink	Downlink	
GSM 850	824.0 … 849.8	869.0 … 894.8	0.1
GSM 900	890.0 … 915.0	935.0 … 960.0	
DCS 1800	1710.0 … 1785.0	1805.0 … 1880.0	
PCS 1900	1850.0 … 1910.0	1930.0 … 1990.0	
UMTS I	1710 … 1785	1805 … 1880	2.8
UMTS II	1850 … 1910	1930 … 1990	
UMTS III	1920 … 1980	2110 … 2170	
Bluetooth	2402 … 2480		0.5
DECT	1880 … 1980, 2010 … 2035		0.868
IEEE 801.11b/g	2400 … 2485		10

Section 2 covers the homodyne architecture sensitivity to static DC offsets and 1/*f* noise, while Section 3 explains the dynamic offset generation in the presence of second order distortions. In Section 4, the best method to avoid self mixing process is presented.

Finally, Section 5 concludes the paper by presenting an updated block schematic of the Fig. 1 receiver that meets the goal of implementing a multi-standard monolithic receiver.

2. Static Offset Compensation

Low DC offset, or 1/*f* noise, values are required for proper signal demodulation during the receiving phase. In practice these low values are not get easily without calibration.

Wireless communications are burst communications and a dedicated time slot for calibration is foreseen: the guard band. Thus, static offset cancelation is possible before each actual receive burst.

While the LNA is AC coupled to the mixer, the mixer output is DC coupled to the baseband part of the Fig. 1 receiver. One of the possibilities to calibrate the receiver static DC offset is the use of the correlated double sampling technique, [3].

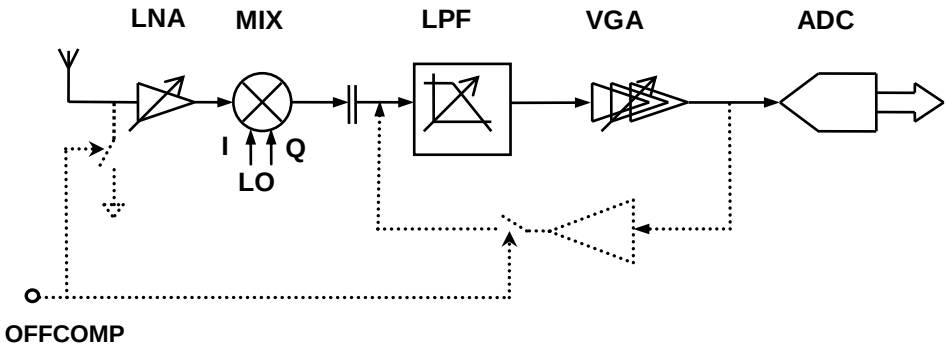

Fig. 2 – Receiver block schematic with analog offset compensation.
(only one baseband channel is shown).

This analogue technique, described by Fig. 2, implies in a first phase (OFFCOMP @ "High" – switches closed) sampling the baseband chain DC offset on a capacitor, via the additional transimpedance amplifier, while the antenna input is shorted to ground.

During normal operation, the second phase (OFFCOMP @ "Low" – switches open), the RF input is connected back to the antenna and the signal flows through the receiver, while the DC offset is inherently cancelled out. In this way, the baseband blocks $1/f$ noise will also be cancelled.

The frequency of two phases alternation is set by the baseband signal bandwidth: the smaller the baseband signal bandwidth the higher is the duration of the DC offset sampling (see Table 1).

The advantage of this technique is the $1/f$ noise is also reduced, next to the static offset cancelation; the drawback is the white noise level doubling because of the aliasing.

Hence, in order to reduce the increase of the wideband noise, for standards with a larger baseband bandwidth, regular AC coupling can be used for the LPF, while the DC offset compensation can be applied only to the VGA.

3. Handling Dynamic Offset

During the receiving period, the RF input power may change significantly, as the other transmitters in the receiver's neighborhood start to transmit a burst. The receiver's even order distortions will change the received signal DC offset component. This *dynamic offset* effect disturbs the received signals demodulation, especially if the envisaged modulation concentrates a large part of the symbol spectral power at low frequency.

Although, the latest wireless standards use modulation schemes that do not require the preservation of the signal DC energy (i.e. IEEE 802-11 – WiMAX), this is not the case for older standards like GSM, for instance.

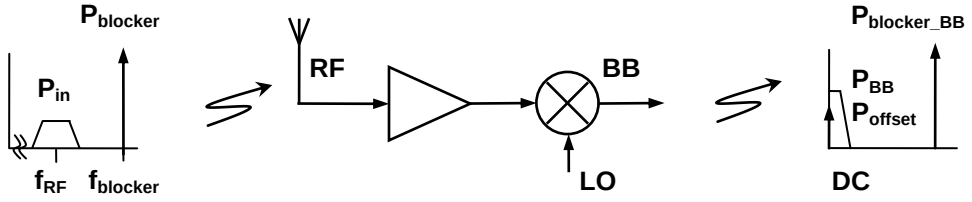

Fig. 3 – DC offset generation due to receiver second order non-linearity.

The presence of second order non-linearity in a receiver generate, while receiving a signal carried on the RF frequency, a DC component as well as a tone at the double of the RF frequency. Fig. 3 depicts a generic situation for the effects of the second order distortions on the receiver output. Basically, next to the very small useful RF signal the receiver is exposed to a very large blocker. As the blocker presence or, respectively, the moment of its appearance are completely orthogonal to the RF signal broadcasting, due to second order non-linearity the receiver output DC level will be larger, or, respectively, change.

The figure of merit quantizing the analog front-end second order distortions is the second order intercept point, *IP*2. Following the representation of Fig. 3, from immediate calculation, the input referred *IP*2 is given by:

$$iIP2 = 2 \times P_{blocker} - P_{in} + \left(P_{BB} - P_{offset}\right), \tag{1}$$

where $P_{blocker}$ is the power of the blocker at the receiver input, P_{in} and P_{BB} represent the useful RF signal power at the receiver input and output and P_{offset} is the DC level of the second order intermodulation product.
Eq. (1) imposes a restriction on the maximum level for the offset component stemming from the second order intermodulation:

$$P_{BB} - P_{offset} \geq SNR_0, \tag{2}$$

where SNR_0 is the minimum Signal-to-Noise Ratio at the receiver ADC output required for the digital demodulator to demodulate the useful signal within the specified Bit Error Rate (BER). Thus, eq. (1) translates to:

$$iIP2 = 2 \times P_{blocker} - P_{in} + SNR_0 \tag{3}$$

For each wireless communications standard a *receiver blocker diagram* is specified, [2]. The diagram consists of all blockers and interferers present at receiver's antenna input, under which influence the receiver must be able, still, to successfully demodulate the wanted signal.

Based on the specified blocker diagram analysis for the targeted standards, it results the worst case scenario is the GSM standard which requires a receiver *IIP*2 of +64 dBm, [4].

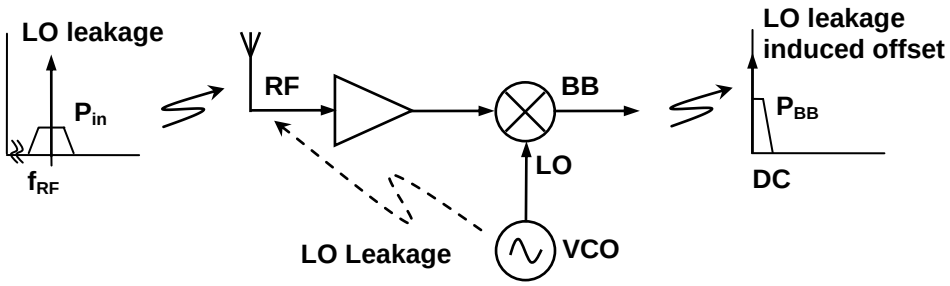

Fig. 4 – DC offset generation due to self-mixing.

The second order and, in general, even order distortions can be dramatically reduced, ideally cancelled, by using *differential circuits*. In order to achieve such high *IIP*2 values the receiver should be implemented by fully differential blocks.

4. Reducing Self-Mixing

The self mixing process occurs when the large swing LO signal, originating directly from the VCO, leaks to the antenna input, gets amplified by the LNA and gets mixed with itself in the downconverter, as shown in Fig. 4.

Hence, a large DC offset is produced at the mixer output. Subsequently, this may eventually clip the receiver output due to the large gain of the receiver baseband chain.

In order to overcome this issue, the VCO must not oscillate at the same frequency with the RF carrier frequency. Hence, the quadrature LO signals driving the downconverter mixer must be obtained by dividing down the VCO frequency.

In order to generate good quality quadrature LO signals over a wide frequency band, the best option, relative to a multi-standard implementation, is to use a Johnson counter, [5]. For such quadrature generators, the VCO frequency must be twice of the desired LO frequency (3…6 GHz), [6]. These circuits are in-deep analyzed in [7].

The DC offset due to self mixing is of same nature with the static offset, since it is only conditioned by the presence of the LO signal and not by the input signal. Thus, it can be calibrated out if the DC offset compensation loop is applied to the mixer's baseband stage as well.

5. Conclusions

This paper analysed the homodyne receiver architecture key issues relative to the monolithic integration in a re-configurable multi-standard radio transceiver. By implementing a DC offset compensation loop, the receiver static DC offset, and inherently $1/f$ noise, are calibrated out during the guard band.

The dynamic offset is made negligible by implementing a fully-differential receiver chain which offers a high *IIP*2. The self-mixing effects are alleviated by using a VCO oscillating at a different frequency than the RF carrier frequency and wide-band frequency dividers to generate the quadrature LO signals.

Based on the presented analysis, Fig. 5 depicts the homodyne radio receiver block schematic ready for monolithic integration in a re-configurable multi-standard radio transceiver.

The multi-standard receiver incorporates 4 wide-band LNAs to be able to deal with the wide-frequency band covering the wireless standards array (see Table 1). The proposed receiver implementation of Fig. 5 has the general characteristics specific to a true multi-standard solution.

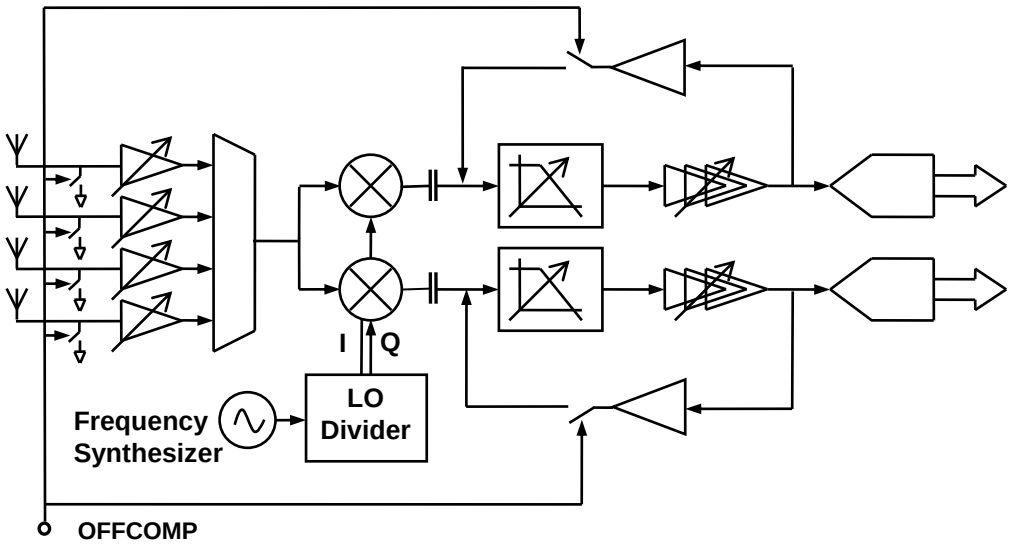

Fig. 5 – Multi-standard homodyne receiver block schematic.

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