Annals of the Academy of Romanian Scientists
Series on Science and Technology of Information
ISSN 2066 - 8562 Volume 3, Number 2/**2010**

MAKING HOMODYNE RECEIVERS READY FOR MONOLITHIC INTEGRATION IN MULTI-STANDARD WIRELESS TRANSCEIVERS

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Abstract. *This paper examines the main issues of homodyne receiver architecture with respect to its monolithic integration in a multi-standard wireless transceiver. The paper's main goal is to find out the architectural changes required to reduce the sensitivity of the zero-IF receiver topology to DC offsets and self mixing process. Based on the presented analysis, the receiver must foresee a DC offset calibration loop and high frequency wide-band frequency dividers in order to facilitate the monolithic integration of the direct conversion architecture, the most suited architecture for a re-configurable multi-standard radio receiver. The paper emphasizes the general character of the proposed implementation, as it fits best a true re-configurable multi-standard implementation.*

Keywords: Software Defined Radio, Direct Conversion Receiver, Receiver Sensitivity, DC Offset Compensation, Dynamic Offset

1. Introduction

The homodyne quadrature down-converter architecture provides the optimum solution for the implementation of Re-Configurable Multi-Standard Radio Receivers, [1]. First of all, in direct conversion receivers the useful signal is its own image: therefore, there is no image to reject and hence no need for an additional image rejection filter. Furthermore, all baseband processing, like analogue filtering, baseband amplification, analog-to-digital conversion and the digital demodulation, take place at the lowest possible frequency. These features make the homodyne receiver an ideal candidate for monolithic integration.

The homodyne receiver block schematic is presented in Fig. 1. The received RF signal is amplified by the low noise amplifier (LNA), then downconverted directly to baseband by mixing with a local oscillator (LO) signal of the same frequency. After the mixer, the baseband signal is filtered by the anti-alias Low Pass Filter (LPF). Subsequently, the Variable Gain Amplifier (VGA) boosts the signal such as the Analog-to-Digital Converter (ADC) to be optimally loaded.

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