Annals of the Academy of Romanian Scientists
Series on Science and Technology of Information
ISSN 2066 - 8562 Volume **3**, Number **2/2010**

LOW CURRENT REFERENCES WITH SUPPLY INSENSITIVE BIASING

Vlad ANGHEL[1], Gheorghe BREZEANU[2]

Abstract. *A comparison between three low current, self-biased current references, in two different configurations, is presented. Channel length modulation effects are taken into account in order to obtain the current dependence on the power-supply voltage variation. Analytical predictions are validated by comparison with simulated curves and measurement data. Moreover, sensitivity is considered, as a design parameter to describe power-supply voltage change effect on the reference output current.*

Keywords: IC (integrated circuit), self-biasing, low current mirrors, Widlar configuration

1. Introduction

Current references are among the most popular block because they are widely used in IC biasing [1]–[7]. Furthermore, as the microelectronic industry is becoming ever more competitive, power consumption is now a main concern. Currents in the range of microamps and less are required in a variety of the applications in order to minimize power dissipation. Such low currents can be generated with current mirrors, in which the transistors operate with unequal gate-source voltage. In addition, the use of self-biasing techniques dramatically increases the output current's independence to power-supply variations.

This paper is focused on three low current mirrors with self-biasing. The performance of these references is described by simulations, analytical models and measurements. The expressions of the sensitivity of the output current to power-supply voltage variations are obtained for the first time.

2. Low current references

One of the most widespread low current mirrors uses a Widlar configuration. In this scheme a moderate resistor is inserted in series with the output transistor of a simple mirror as shown in Fig. 1 [6]. Moreover, the circuit is less sensitive to the input current and the supply voltage than the simple current mirror. A first view analysis of the Widlar current reference starts with the loop consisting of M_1, M_2 and R_2:

$$V_{GS1} - V_{GS2} - I_{OUT}R_2 = 0 \qquad (1)$$

[1]Ph.D., Eng. University "Politehnica" of Bucharest, Romania, vlad.anghel@onsemi.com.
[2]Prof. univ. Ph.D., University "Politehnica" of Bucharest, Romania. Corresponding member of the Academy of Romanian Scientists; gheorghe.brezeanu@dce.pub.ro.