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AN OVERVIEW OF THE KEY FEATURES OF FREQUENCY SYNTHESIZERS ARCHITECTURE USED IN MULTI-STANDARD MONOLITHIC TRANSCEIVERS

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Rezumat. *Lucrarea analizează arhitecturile sintetizoarelor de frecvenţă utilizate în transiverele reconfigurabile de bandă largă, urmărind identificarea unei arhitecturi optime pentru sintetizatorul de frecvenţă, ţinând cont de particularităţile proiectării de radiofrecvenţă. Lucrarea descrie atât topologia cât și particularităţile blocurilor componente circuitului care satisface cerinţele stricte ale aplicaţiilor wireless. Acest deziderat este realizat de sintetizorul de frecvenţă fracţionar bazat pe un oscilator LC de bandă largă, comandat în tensiune. Lucrarea prezintă arhitectura sintetizorului de frecvenţă fracţionar, descrierea și analiza principalelor aspecte legate de implementarea acesteia.*

Abstract. *This paper presents the analysis on frequency synthesizer architectures used in multi-standard re-configurable wide-band transceivers, focused on finding the optimum frequency synthesizer architecture, given the wide-band RF design specifics. The paper describes both the circuit's topology and specifics of circuit's building blocks that mitigate the stringent requirement of wireless applications. The architecture of the fractional-N frequency synthesizer based on a wide-band frequency range LC Voltage Controlled Oscillator (VCO), that accomplishes this task, is presented and its key design features are described and analyzed.*

Keywords: Multi-Standard Radio Transceiver, Frequency Synthesizer

1. Introduction

The common architecture of a multi-standard reconfigurable wide-band transceiver is the quadrature direct conversion RF front-end, see Fig. 1, [1]. The receiver (RX) is a zero-IF downconverter. The RF signal is amplified by the Low Noise Amplifier (LNA) and downconverted to the baseband by mixing with a Local Oscillator (LO) signal having the same frequency, in the mixer (RXMIX) block. Subsequently, the RX Low Pass Filter (RXLPF) provides the analog channel selection, removing all out-of-band blockers and interferers. Finally, the Variable Gain Amplifier (RXVGA) boosts the wanted signal providing the optimal RX Analog to Digital Converter (RXADC) loading.

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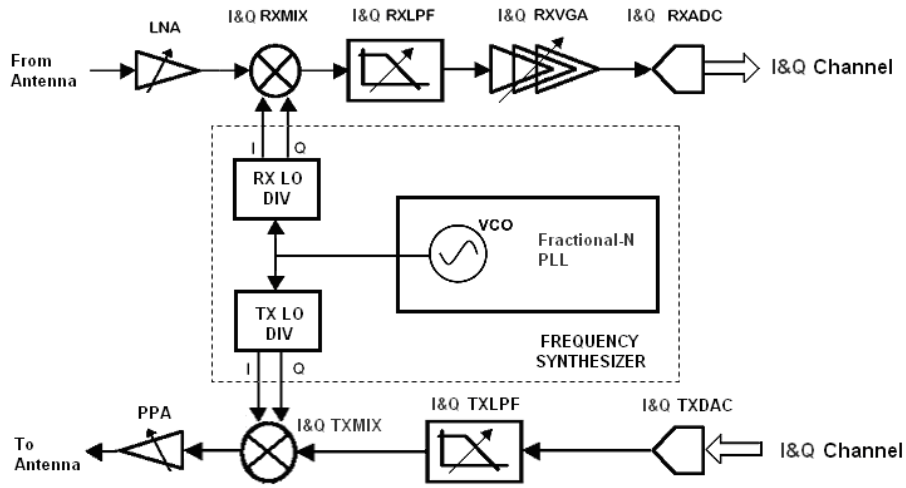


Fig. 1. Software Re-configurable Radio Transceiver.

The transmitter (TX) converts the digital input stream to analog by means of the TX Digital to Analog Converter (TXDAC). The anti-aliasing TX Low Pass Filter (TXLFP) filters out the spectral replicas inherent to any digital-to-analog conversion. The homodyne quadrature image rejection mixer (TXMIX) upconverts the conditioned analog signal directly on the desired frequency by mixing it with a Local Oscillator (LO) signal having the same frequency. The Pre-Power Amplifier (PPA) acts as a buffer for the TX chain; its task is to drive the off-chip Power Amplifier or directly the antenna. The "heart" of the Software Re-configurable Radio Transceiver in Fig. 1 is the frequency synthesizer. Its beat is represented by the LO signals that allow up- or down-conversion of the wanted signal. Table 1 presents the major wireless standards center frequencies. The frequencies of interest cover a wide range spanning from 800 MHz to about 3 GHz.

Fig. 2 presents the typical frequency synthesizer block schematic. Basically, the frequency synthesizer is a programmable Phase Locked Loop (PLL) circuit. Given the small channel spacing of various wireless standards (see Table 1), a fractional-N divider is the optimal choice for a software reconfigurable radio transceiver. The selection of receiving or transmitting channel is realized by tuning the Voltage Controlled Oscillator (VCO) frequency to the appropriate value.

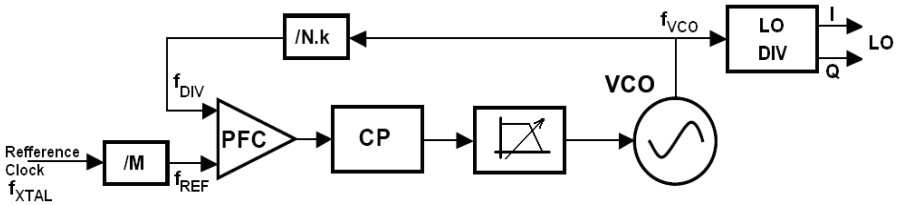


Fig. 2. Frequency synthesizer block schematic.

Table 1

Major Wireless Standards
Frequency Plan and Maximum Baseband Channel Bandwidth

Wireless Standard	Frequency Plan [MHz]		Maximum Baseband Bandwidth [MHz]
	Uplink	Downlink	
GSM 850	824.0 ÷ 849.8	869.0 ÷ 894.8	0.1
GSM 900	890.0 ÷ 915.0	935.0 ÷ 960.0	
DCS 1800	1710.0 ÷ 1785.0	1805.0 ÷ 1880.0	
PCS 1900	1850.0 ÷ 1910.0	1930.0 ÷ 1990.0	
UMTS I	1710 ÷ 1785	1805 ÷ 1880	5.0
UMTS II	1850 ÷ 1910	1930 ÷ 1990	5.0
UMTS III	1920 ÷ 1980	2110 ÷ 2170	5.0
Bluetooth	2402 ÷ 2480		0.5
DECT	1880 ÷ 1980, 2010 ÷ 2035		0.6
IEEE 801.11b/g – Wi-Fi	2400 ÷ 2485		5.5
IEEE 802.16e - WiMax	2.3÷ 2.5, 3.4÷ 3.5		10.0

The VCO frequency, F_{VCO}, is given by

$$F_{VCO} = N.k \times F_{XTAL} / M = N.k \times F_{REF} \quad (1)$$

where F_{XTAL} is the quartz oscillator (XTAL) reference clock frequency, M the F_{REF} division ratio, and $\boldsymbol{N.k}$ the fractional loop divider division factor.

The transceiver of Fig. 1 is a quadrature one. In order to generate good quality quadrature LO signals over a wide frequency band, the best option is to use a Johnson counter, [2]. For such quadrature generators, the VCO frequency must be twice of the desired LO frequency (3…6 GHz, see Table 2). Thus, the frequency synthesizer uses two programmable LO divider circuits (LODIV), one for RX and the other one for TX; these circuits are in analyzed in detail in reference [3].

In Section 2 the PLL phase noise impact on both the RX and TX performance is analyzed. In Section 3, the main phase noise contributors are presented, and the key trade-off in PLL design for wireless applications is defined: *the trade-off between noise performance and locking speed*. Section 4 overviews the common VCO topologies and proposes the best solution for a low phase noise PLL. In Section 5 the loop filter performance is assessed in order to select the filter order that optimally mitigates the transient loop response and reference spurs suppression, without degrading the loop's phase noise. Finally, Section 6 concludes the paper by reviewing the proposed architecture.

Table 2

VCO Tuning Range and LO Frequency Ranges

VCO Tuning Range	LODIV Division Factor	LO Frequency
3…6 GHz	/2	1.5…3 GHz
3…6 GHz	/4	0.75…1.5 GHz
3…6 GHz	/8	0.375…0.75 GHz

2. PLL Phase Noise Impact on Transceiver Performance

From the RF design perspective, the main parameter of the PLL circuit is the phase noise, measured in dBc/Hz. The phase noise measures how much of the carrier energy is dispersed around it. The time domain phase noise equivalent is the jitter, which represents a measure of the oscillation frequency precision. From the phase noise perspective there are two potential dangers for the Fig. 2 frequency synthesizer. One is related to the receiver, while the other one to the transmitter.

PLL Phase Noise Impact on the Receiver

While receiving, due to the LO signal noise "tail", the receiver downconverts a fraction of the signals located in the adjacent channels. Hence, at the mixer output the downconverted unwanted signals will overlap on top of the useful signal, thus decreasing the receiver Signal-to-Noise Ratio (SNR):

$$SNR_{PN} = SNR - PN \times Blocker\,[dB], \tag{2}$$

where the SNR_{PN} represents the in-band SNR in the presence of phase noise, *PN* is the LO phase noise at the blocker frequency measured in dBc/Hz and *Blocker* is the power level of the un-wanted signal picked up by the LO signal tail. This way the quality of the digital demodulation process, described by the *Bit Error Rate* (BER) is worsened. For various digital modulation schemes a given BER is obtained for a certain receiver SNR, as detailed in [4]. For each wireless communications standard a receiver blocker diagram is specified. The diagram consists of all blockers and interferers present at receiver's antenna input, under which influence the receiver must be able, still, to successfully demodulate the wanted signal. Knowing the required SNR that allows a proper demodulation of the received signal and the receiver blocker diagram, eq. (2) allows the calculation of the frequency synthesizer's phase noise requirements during the receive phase, [5].

PLL Phase Noise Impact on the Transmitter

While transmitting the LO noise tail or other spurious generated by the frequency synthesizer will pollute the output transmit spectrum. This may cause interference with other transceivers. In order to prevent such interference each wireless standard specifies the transmit output spectral density mask. From this mask the transmit phase noise requirements are derived straight forward, [5].

3. The Key PLL Trade-Off: Phase Noise vs. Transient Performance

In this Section the major phase noise contributors will be analyzed: the reference clock and the VCO. In order to assess their contribution to the total PLL output phase noise, the close-loop response must be analyzed. The PLL can be represented as a negative feed-back system in frequency, see Fig. 3.

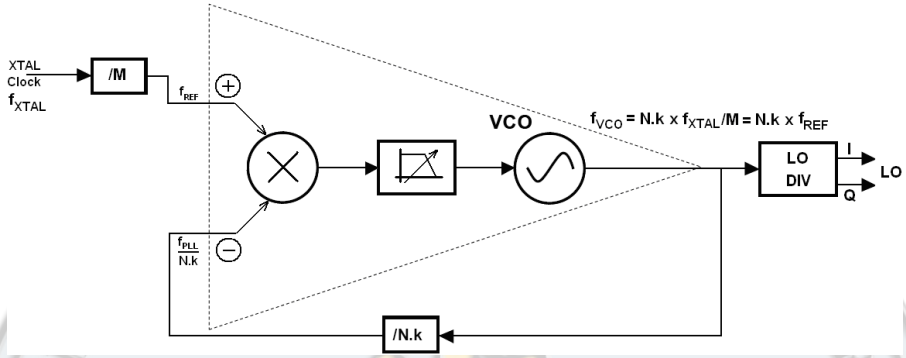


Fig. 3. PLL viewed as a negative feed-back system in frequency.

Taking into account a PLL that uses a phase detector without charge pump, the system close loop response is given by:

$$F_{VCO}/F_{REF} = M \times a/(1+a\beta), \tag{3}$$

where a is the forward open-loop gain and β is the feed-back factor:

$$a(s) = K_{PFC} \cdot K_{LPF}(s) \cdot K_{VCO}(s), \ \beta = 1/N.k, \tag{4}$$

with K_{PFC} the PFC gain, $K_{LPF}(s)$ the loop filter transfer characteristic and $K_{VCO}(s)=K_{VCO}/s$ the VCO sensitivity. For a strong negative feed-back, $a\beta >> 1$, the close loop response is given by eq. (1). If the loop filter has a constant transfer characteristic, $K_{LPF}(s) = K_{LPF}$, the open loop transfer function becomes:

$$a\beta = K_{PFC} K_{LPF} K_{VCO}/N.k \cdot s = K_F/N.k \cdot s, \tag{5}$$

where K_F is the loop gain measured in s^{-1}.

Equation (5) describes a first order PLL, which exhibits one pole in the origin due to VCO. The calculated reference phase noise, PN_{REF}, and the VCO phase noise, PN_{VCO}, contributions to the PLL phase noise, PN_{PLL}, are given by:

$$\begin{cases} PN_{PLL}/PN_{VCO} = 1/|1+a\beta|^2 = |s/(s+\omega_c)|^2 \\ PN_{PLL}/PN_{REF} = |a/(1+a\beta)|^2 = N.k^2\omega_c^2/|s+\omega_c|^2 \end{cases}, \tag{6}$$

where PN_{VCO}, PN_{REF} and PN_{PLL} represent the phase noise spectral density measured in dBc/Hz and ω_c is the loop cross-over frequency, or the frequency at

which the open loop gain has a magnitude equal to one:

$$\omega_c = K_F / N.k \tag{7}$$

Hence, the total noise contribution at the PLL output becomes:

$$PN_{PLL} = PN_{REF} \cdot N.k^2 \omega_c^2 / |s + \omega_c|^2 + PN_{VCO} \cdot |s/(s + \omega_c)|^2 \tag{8}$$

The loop response is low pass type for PN_{REF}, and high pass type for PN_{VCO}. The 3-dB cut-off frequency of these characteristics is ω_c, see Fig. 4.

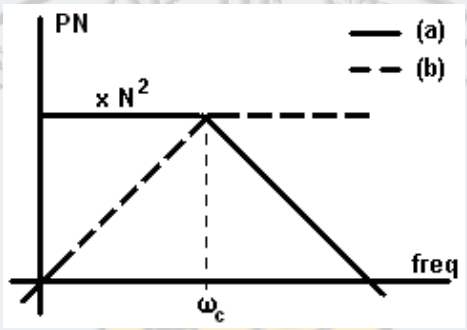


Fig. 4. PLL phase noise characteristic towards: (a) Reference noise and (b) VCO noise

The loop rejects PN_{VCO} for small frequency offsets around the center oscillation frequency, as opposed to amplifying PN_{REF} by N^2. For frequency larger than ω_c, the loop suppressing action towards PN_{VCO} fades-out and increases towards the XTAL phase noise with a slope of 20 dB/dec. In PLL design for wireless applications the key trade-off is between the phase noise performance and the loop transient response: the higher is ω_c, the smaller is the locking time, but more in-band noise is injected from the XTAL reference; while the smaller is ω_c, the PLL locks slower, but less reference noise is amplified to the output.

4. VCO Choice

The phase noise of a VCO has three well-known regions according, [6], to the characteristics plotted in Fig. 5.a. In the first region the PN_{VCO} varies as ω^{-3} due to the non-linearity of the devices used to build the VCO, which up-convert the low-frequency $1/f$ noise to the carrier frequency. In the second region, the PN_{VCO} exhibits a decrease with ω^{-2}. This derives from the amplification, due to the oscillator positive feed-back, of white noise sources located around the center oscillation frequency. And, finally, at high frequency offsets white noise prevails.

Within the PLL bandwidth, the VCO phase noise is filtered out, while for frequencies larger than ω_c, the same phase noise gets directly at the PLL output, resulting the total PLL phase noise plot of Fig. 5.b. Table 3 summarizes all oscillator types with respect to the low phase noise requirement, [6].

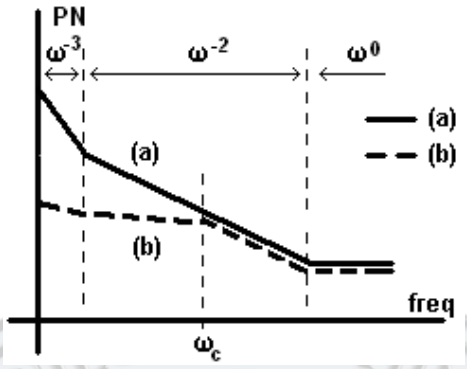


Fig. 5. Typical VCO Phase Noise, (a), and PLL Total Phase Noise, (b).

Table 3

Oscillator Types vs. Phase Noise Performance

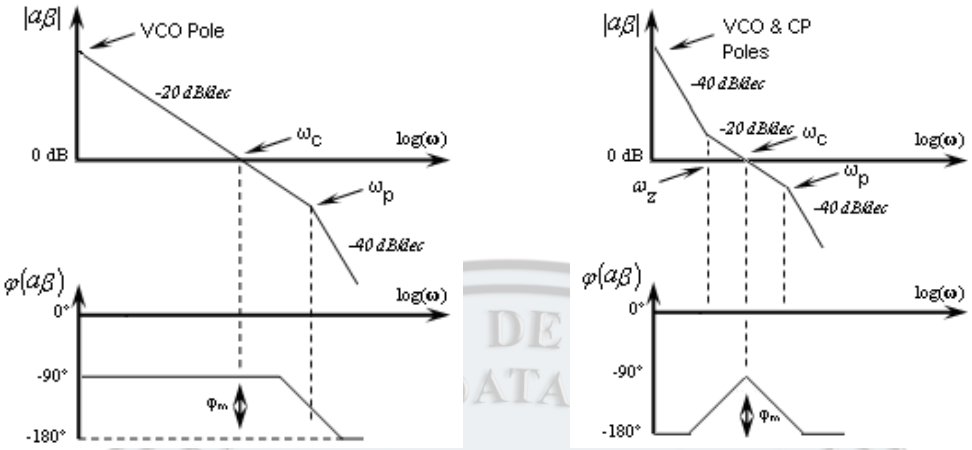
Oscillator Types	Typical Frequency Range	Phase Noise Considerations
Gm-C	Up to a few hundered MHz	Bad phase noise and spurious spectrum
Relaxation	Up to a few GHz	Low phase noise with large power consumption
Ring	Up to a few dozen GHz	Bad phase noise performance
LC	Up to a few dozen GHz	Low phase noise due to passive elements

It results the only viable solution for a PLL used in mobile wireless application is the LC-VCO.

The LC oscillator has also another advantage: given the low values of the integrated spiral inductors that render its high oscillation frequency, the LC-VCO offers even a lower phase noise if the targeted application uses a carrier located at a frequency lower than half the VCO frequency. Each division by 2 of the LO frequency halves its phase noise. Hence, after a division by 2 the LO signal of the up- or down-conversion mixer will have 6 dB less phase noise.

5. LPF Order Impact on the PLL Transient Response.

The Loop Filter optimizes the PLL's noise and transient behavior, by introducing poles and zeroes in the loop's transfer function, and provides additional suppression of the reference frequency harmonics. In order to get a better suppression of the reference frequency harmonics, generated by the phase-frequency comparator, and faster locking time, an extra pole, ω_p, is required, see Fig. 6.b; the PLL became a second order system, and the stability may be an issue. Enough phase margin must be considered to avoid an oscillatory close loop response or a large overshoot when the loop changes its oscillation frequency. This is why ω_p has to be larger than ω_c, see Fig. 6.b; e.g. for 45° phase margin $\omega_p = \omega_c$, [7]. The new filter and loop transfer functions are shown in Table 4.



a. b.

Fig. 6. Bode Characteristics for: a. Second Order PLL b. Third Order Charge Pump PLL.

Table 4

Second and Third Order PLL Transfer Characteristics

	Block	Transfer Characteristic
Second Order PLL	LPF	$K_{LPF}(s) = K_{LPF} / (1 + s/\omega_p)$ - ω_p the active/passive LPF pole frequency
	CLOSE LOOP	$\frac{F_{VCO}}{F_{REF}}(s) = \frac{a(s)}{1 + a(s)\beta} = \frac{\omega_p K_F}{s^2 + \omega_p s + \omega_p \cdot K_F / N.k} = \frac{\omega_p K_F}{s^2 + 2\xi\omega_n s + \omega_n^2}$ - $K_F = K_{PFD} \cdot K_{LPF} \cdot K_{VCO}$, the forward loop gain - $\omega_n = \sqrt{\omega_p \omega_c}$, the PLL natural frequency - $\xi = 0.5\sqrt{\omega_p / \omega_c}$, the damping factor
Third Order PLL	LPF	$K_{LPF}(s) = [1 + s/\omega_z] / s(C_p + C_z)(1 + s/\omega_p)$ - $\omega_p = (C_p^{-1} + C_z^{-1}) / R_z$, the passive LPF pole frequency - $\omega_z = (R_z C_z)^{-1}$, the passive LPF zero frequency
	OPEN LOOP	$a\beta = [K_{PFD-CP} \cdot K_{VCO}(s) \cdot K_{LPF}(s)]\beta = \frac{1}{s/\omega_c} \cdot \frac{1 + s/\omega_z}{(1 + s/\omega_p) \cdot s/\omega_z}$ - $\omega_c = (K_F / N.k) \cdot [R_z C_z / (C_p + C_z)] = 0.25\,\omega_p / \xi^2$, the cross-over freq. - $K_F = K_{PFD-CP} \cdot K_{VCO}$, the forward loop gain

By adding an extra-pole at low-frequencies, thus turning the loop into a third order one, its transient response is further improved, [8]. Due to the extra phase shift of 90°, a zero must be place to ensure sufficient phase margin.

In practice, for monolithic PLLs a charge pump is used, because of the more relaxed and efficient implementation.

In addition to the existing VCO pole, the charge pump adds another one, also in the origin, due to the high-impedance state of its output when the loop is locked, [9]. The loop filter schematic for a third order charge pump PLL is depicted in Fig. 7, while Table 4 notes the new filter and third order open loop PLL transfer functions.

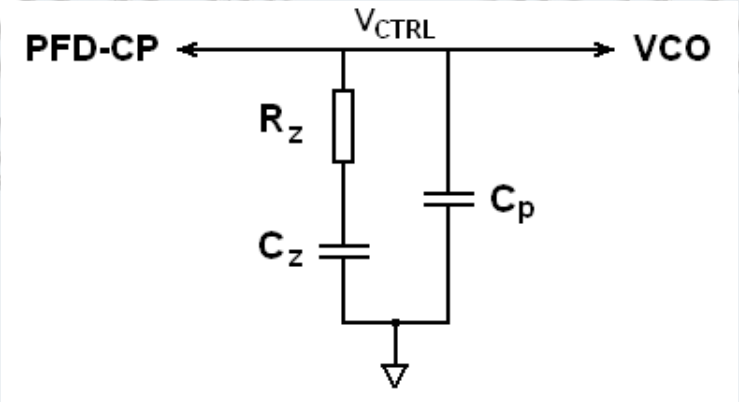
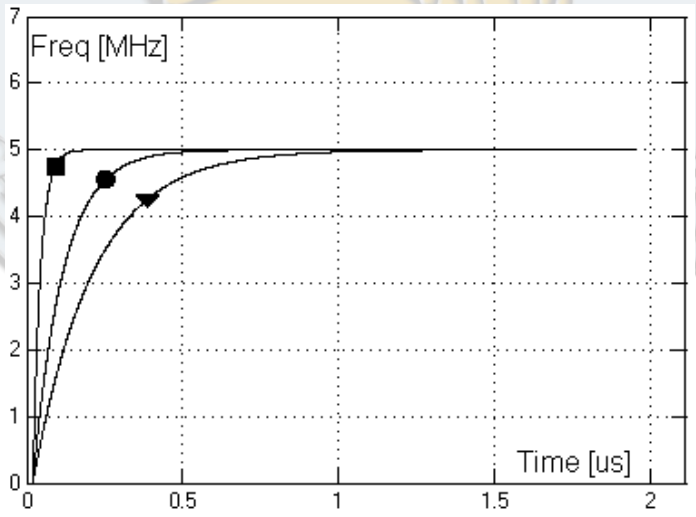
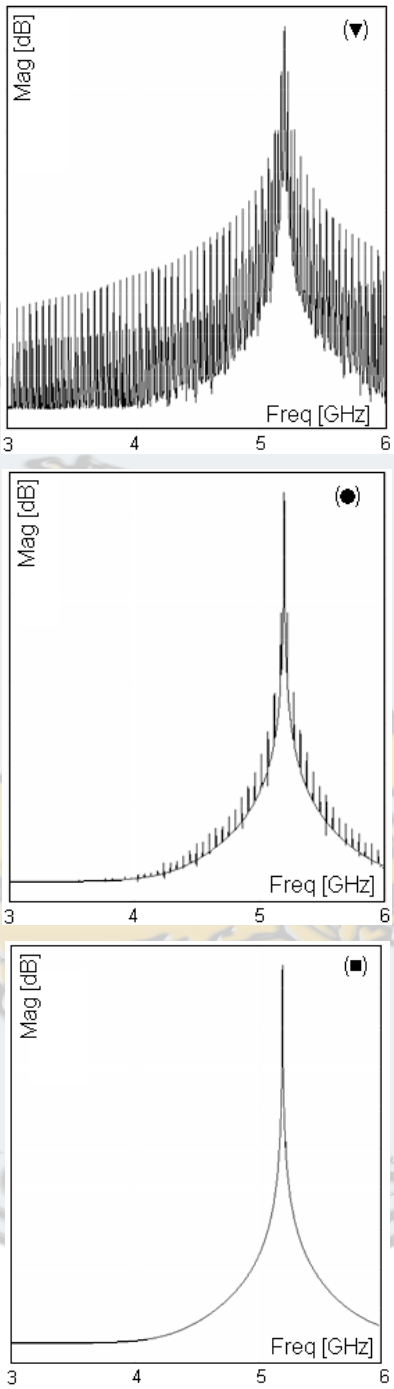


Fig. 7. Loop Filter for Third Order Charge-Pump PLL.



a.

Fig. 8. a. Loop Transient Response:
▼First Order PLL, ● Second Order PLL and ■ Third Order PLL.



b.

Fig. 8. b. Output Spectrum:
▼First Order PLL, ● Second Order PLL and ■ Third Order PLL.

The transient loop response for the three PLL orders has been simulated for an output frequency of 5 GHz generated from an XTAL reference frequency of 26 MHz a division factor of 192.3.

The same loop bandwidth of 200 kHz was considered for all three cases. Moreover, the second and third order PLLs were designed to have the same 70° loop phase margin.

As expected the third order PLL offered the fastest locking time, as shown Fig. 8.a. Also, for higher PLL orders, the filtering of reference frequency and its harmonics improves substantially, as depicted in the comparison of Fig. 8.b.

The plots show the output spectrum of the PLL operating in integer mode: 5.2 GHz output frequency generated from a 26 MHz XTAL and an integer division ratio of 200.

Conclusions

This paper presented the analysis of the most suited frequency synthesizer architecture for multi-standard re-configurable wide-band transceivers.

The fractional-N frequency synthesizer based on a high oscillation frequency, wide-band frequency range, LC VCO, guarantee best phase noise performance, while maintaining a fast locking time.

The impact of the synthesizer phase noise on both the receiver and the transmitter has been presented.

The key noise contributors, the VCO and the XTAL reference, have been analyzed and their noise contributions to the PLL's total phase noise have been calculated.

Finally the key trade-off in PLL design for wireless applications, the trade-off between noise performance and locking speed, was assessed by checking the loop LPF order impact on the PLL transient response.

By implementing a second order filter, the third order charge pump PLL offers the fastest locking time compared to a lower order PLL, while improving the reference spur rejection.

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