Annals of the Academy of Romanian Scientists
Series on Science and Technology of Information
ISSN 2066-8562 Volume **3**, Number **1**/**2010**

FROM 2D MICROELECTRONICS TO 3D MICROSYSTEMS

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Rezumat. *Lucrarea face o scurtă trecere în revistă a evoluției electronicii integrate pe siliciu de la tehnologia planară (2D) până către zorii tehnologiei 3D, luând ca referință predicțiile formulate de Gordon Moore în 1965 privind dublarea numărului de componente pe cip a circuitelor integrate la fiecare 12 luni, aplicațiile prezise dar și provocările științifice și tehnice lansate de același autor în vederea îmbogățirii funcțiilor electronice realizabile pe cip. Lucrarea va evidenția validitatea de peste 4 decenii a legii lui Moore sub sintagma „More Moore" și modul în care, în ultimii ani, aceasta tehnologie 2D se suprapune cu apariția tehnologiei 3D de microsistem denumită „More than Moore" prin care pe chip-ul 3D se procesează semnale electrice și neelectrice și se transmit fără fir la centre de decizie. Un exemplu de aplicație dezvoltată pe un chip 3D un la nivel virtual de către Honeywell este arătat ca un studiu de caz.*

Abstract. *In this paper we shall briefly review the evolution of the silicon integrated electronics from the planar technology (2D) till the early stages of 3D integrated technologies, taking as a reference the Gordon Moore's predictions from 1965, of doubling on-chip IC components every 12 months, his envisaged applications, as well as the scientific and technical challenges launched by Moore for enhancing the on-chip electronic functions. The paper will evidence the validity of Moore's law after more than 4 decades, under the collocation of „More Moore" and the way in which, in the last years, this 2D technology is overlapping with the emerging 3D technology called „ More than Moore" which is processing the electrical and non-electrical signals that are subsequently wirelessly transmitted to the decision taking centres. An example application virtually developed on a 3D chip by Honeywell is shown as a study case.*

Keywords: 2D integrated electronics, 3D integrated technology, behavioral modeling, SAW sensing platform

1. Introduction

Transistor discovery and the invention of the integrated circuit have triggered a tremendous development of the semiconductor material science and technology, where silicon has received the dominant role for both bipolar and MOS technology implementation [1]. The evolution of the silicon-integrated electronics towards increased on-chip functionality was possible thanks to the progress of entire technical environment and advanced clean room environment, on one hand,

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and improved integrated circuit (IC) design methodology on the other hand, with very well understood scaling-down laws for the dimensions of the MOS transistor [2, 3]. A synthetic view of the IC technology development from 1959 till 1965 has given to Gordon Moore enough hints to predict that the 2D integrated electronics will double the number of integrated transistors per chip at every 12 months, at a minimum cost of component per chip [4]. His thorough understanding of the limitations of the IC technology from his time, combined with his vision for future IC-based system applications have created a strong foundation and a scientific and technical challenge for the international technology roadmap for semiconductor (ITRS) for more than four decades.

Down the road predicted by Moore, the bulk-CMOS technology has become rapidly the major platform for the realization of the complex integrated circuits, where the semiconductor dynamic random access memories (DRAM) memories and microprocessors have increased their complexity from the 1KB memory and "4004 microprocessor" family in 1972 to 4GB memories and "Pentium 4 microprocessors" at 2.4 GHz from nowadays [5]. In terms of the technology roadmap, the dimensions of the bulk-CMOS transistors decreased from a channel length of 10 μm in 1970 to 66 nm in 2006, while the predictions are that the channel length will reach 14 nm in 2020, which appears to be the end of the roadmap for bulk CMOS technology evolution. This period of progress beyond the critical dimension of 130 nm, is associated to the nano-electronics domain and is called "More Moore" because the Moore's law of increased complexity as a function of time is still valid. The "show stopper" for the bulk-CMOS devices and technology are the short channel effects which will make impossible the control of the MOS transistor by the gate voltage, due to the increased leakage currents flowing between source and drain as well as tunneling currents between gate and channel, through the gate dielectric [6]. Early, at the large shade of the bulk-CMOS technology, the silicon on insulator (SOI) technology was developed and this was gradually refined until recent years, when the first commercial microprocessor and memories appeared on the semiconductor market [7, 8]. It is the mission of the SOI-CMOS technology to take over the flag of device shrinkage and reduce the transistor channel below 10 nm by using new MOS transistor concepts like dual gate, three gate or all gate around SOI MOSFET transistors [6-7]. These new concepts of transistor called now "finfet" appeared after the discovery of the dual gate MOSFET transistor in 1984 and its proof of concept by Sorin Cristoleanu's team in 1987 [9].

In parallel with above micro and nano-electronics evolution, the domain of miniaturized sensors has been developed, with a main interest on silicon sensors as described in the literature [10, 11]]. The partnership of the IC technology with the sensors technology has led to the integrated sensors domain, where the sensor

and the electronic circuitry for conditioning and processing of the signal coming from the sensor can be located on the same chip, creating the first integrated silicon sensor. The integrated pressure sensor working on the piezoresistive principle is the first example of a commercial 2D integrated microsystem, where mechanical and electrical signals are processed on the same chip. The need for small size complex micro-systems with a large diversification of functions from analog and digital information processing and RF wireless transmission till a broad range of sensing and actuation functions have generated an emerging 3D integrated technology, which is called "More than Moore" able to address these requirements [5]. This vertical integration is the result of assembling together, one over the other, different pre-processed chips, in order to obtain a 3D stack of chips electrically and mechanically interconnected by through-the-chip-vias. Thus, the "More than Moore" 3D integrated technology will open the way to complex micro-nano integrated systems able to interact with people and environment by wired or wirelessly means in order to detect the status of surrounding physico-bio-chemical world and to communicate this info in real-time to a central station or people for taking a decision.

In the above context, the purpose of this paper is to emphasize the technology background existing at the middle of 60' that allowed to Gordon Moore to do his robust predictions for 2D IC complexity growth and for future system applications. Moore has also identified the key device and technology challenges necessary to be addressed in the future for bringing more functions doable on the silicon chip. The motivation for the evolution of the 2D integrated electronics to 3D integrated microsystems will be also described here. Finally, within this paper we shall describe our virtual approach for the structural health monitoring of assets by means of an autonomous, wireless 3D integrated MEMS micro-system.

2. More about Moore and his vision for 2D electronics and applications

The invention of the integrated circuit (IC) concept by Noyce and Kilby at the end of 50" and beginning of 60' has triggered the entire progress of the integrated electronics, which we have seen growing during the last four decades [12,13]. Rapid acceptance by the industry was possible due to low cost and high performance and reliability of integrated circuits, when fabricated at high volume. This IC concept consists of doing on the same piece of silicon (chip) all the active and passive components, which are electrically interconnected by highly conductive films adherent to the substrate and deposited in the same processing sequence. The first integrated circuits were performed in the bipolar technology, where the fluxes of both majority and minority charge carriers (electrons and holes) are determining the electrical currents in the „pnp" and „npn" integrated transistors, but the CMOS technology, which is based on MOS transistor

operating with one type of carriers only has received the largest utilization in both linear and digital integrated circuits, due to mainly its low power consumption for doing the transistor function. Once the IC concept was reduced to practice, the number of electronic components integrated on the same chip has started to grow year by year. Gordon Moore has analyzed the growth of the number of electronic components per chip from the period 1962 and 1964 and from these data he has understood that the component density per chip at minimum cost per integrated component can be doubled at each 12 months [4]. This has thus become the „law of Moore" for 2D integrated electronics growth, which was then followed by more than 4 decades by the commercial fabrication of the IC's. Based on his findings, in 1965 Moore has anticipated that by 1975 the IC would have about 65000 transistors per chip, which was true. Today, the evolution of IC complexity per chip is still following the law of Moore, and it will be kept like this till about 2020 when the physical limitation as short channel effect (SCE) will stop further device miniaturization, for a channel length of the bulk CMOS transistor of about 14 nm. Actually, the downscaling of the Si CMOS transistor below 100 nm, while the velocity of IC complexity per chip is still according to the law of Moore is called „More Moore". From this reason, Gordon Moore could be called the father of the International Technology Roadmap for Semiconductors (ITRS). This long term prediction of the IC complexity increase was possible when Moore realized that there was no fundamental limitation to the scaling down process till the nanometer range.

What is less known about Gordon Moore are his predictions in the field of IC technology and devices, where multilevel metallization separated by dielectric layers are envisaged for the increase of IC complexity and realization of multiple electronic functions per chip, or the extensive use of optical lithography with possible transition to electron lithography for small critical dimensions during scaling down process. At integrated circuit level, he has predicted increased performances of differential integrated amplifiers, integrated RF amplifier with off-chip high Q components , digital filters and miniaturized large semiconductor memories distributed anywhere in the machine. In addition, Moore has envisaged the „explosion" of system electronics, where he mentioned (we remember it was 1965) that home computers, personal portable communication devices and automatic control of automobiles will become a reality in the next decades, and all these magic things became true later.

As important as his predictions are his statements related to the unsolved issues of device and technology which could enhance the functionality of silicon integrated technology. Thus, Moore has shown that the lack of on-chip capacitors (C) and inductors (L) are limiting the capabilities of integrated electronics for analog applications, where the above energy storage components will have to be done by

off-chip passive components, increasing thus the space needed for a certain electronic function. Finally, Moore has challenged the scientific community to find resonant phenomena in silicon devices, like in the case of piezoelectric devices on quartz, in order to perform RF tuning functions which need high quality factors.

Later, the technical solutions for the above bottle necks of 2D microelectronics started to come, once the silicon technology began to dig deep trenches in the silicon body and the Micro-Electro-Mechanical Systems (MEMS) were developed for creating on-chip sensing and actuation functions. Thus, by using the 3D silicon trench technology and high-k dielectrics, recently, a capacitance of 0.4 μF in a silicon area of 1 mm^2 was reported [14]. Similarly, today, RF-MEMS technology is showing that the realization of the low loss, suspended coils for different applications is possible. Moreover, RF-MEMS vibrating capacitive structures excited with an ac electrical signal of frequency equal to the natural resonant mechanical frequency of suspended elements [15] have opened the way to on-chip high-Q resonant devices allowing RF-MEMS based oscillators, which entered the market, recently.

3. More than Moore: From 2D Microelectronics to 3D Microsystems.

Continuous shrinkage of silicon devices allowed more and more electronic functions to be integrated on the same chip reaching the stage of a 2D system- on-chip (SoC). Due to increased functionality of SoC and technology advances, despite the transistor miniaturization, the maximum chip size of such integrated electronic systems performed at minimum cost of on-chip manufactured transistor has continuously increased. However, for a chip size higher than a certain value, the fabrication yields for such a SoC start to decrease, and, therefore, from economical considerations, further electronic functions could not be added on a single SoC. At this point, the 3D technology appeared as a solution to the challenges of the 2D SoC. Thus, further increase of the 2D SoC complexity has become possible only after the concept of vertical integration has been developed and implemented. As a result of the 3D technology development, a microprocessor and associated silicon memory have been already brought to the market, as a single 3D SoC. These 3D integrated systems from above perform pure electronic functions as required by different applications. Without entering the details of the 3D technologies, it is worth to mention here, its specific features, in terms of thinning the wafers, (vertical) stacking and bonding the chips, using inter-chip electrical interconnections called Through the Silicon Vias (TSV).

In parallel with these ”pure” electronic 3D SoC’s, a new family of vertical integrated systems, called 3D Microsystems is growing, where, in addition to the above electronics functions, the sensing and actuating functions, energy

harvesting as well as wireless communications functions can be embedded in the same stack, transforming such a complex component into an autonomous and wireless System-in-Package (3D SiP) for real time control of industrial processes and assets, environment, bio-medical applications. This new field, where the electrical, mechanical, chemical, thermal, optical and magnetic signal can be on-3D-chip processed and wirelessly transmitted from a 3D chip is called „More than Moore" domain. Within „More than Moore" approach, the 3D stack is obtained by bonding one over the other very many 2D chips, while each chip will perform a certain microsystem function. Moreover, chip performed in different technologies and on different types of substrates, can be bonded together for getting a 3D stack performing a certain function. Thus, the 3D stack can contain silicon chips as well as quartz chips, assembled together by specific chip-to-chip or wafer-to-wafer bonding technologies. In the case of wireless 3D-MEM Microsystems, an important role to the minimum size of the 3D stack comes from the antenna size, which will consume less and less area, if the frequency of the RF signal to be converted into electromagnetic signal and the opposite is increasing. Such a 3D stack can be smaller than 1 mm×1 mm×1 mm for RF frequencies higher than 10 GHz, for example. Below, we shall present an example of a complex application, specific to the domain of structural health continuous monitoring of assets (SHCMA), where a 3D technology can be used for the realization of the 3D microsystem that will perform the application requirements.

4. An example of a 3D Microsystem for Asset Monitoring

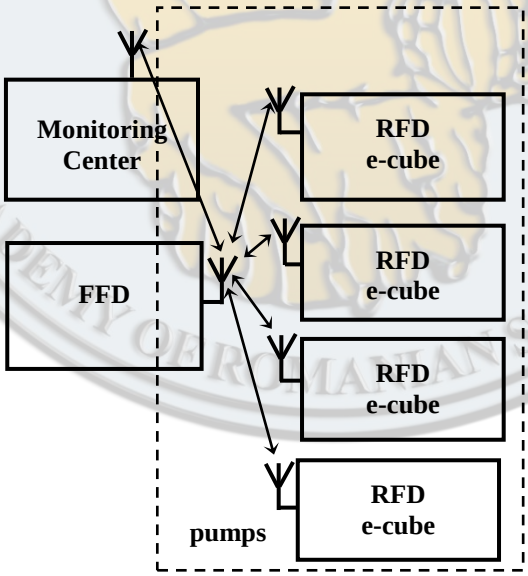

Fig. 1. System level-SHCMA application description

Structural Health Continuous Monitoring of Assets (SHCMA) consists in real-time supervision of the condition (health state) of the components of a system

by means of set of sensors. SHCMA is determining the transition from Scheduled based Maintenance to the Condition Based Maintenance (CBM), which is going to reduce the cost of down time and finally the maintenance, itself. As an example here, we describe a SHCMA application consisting of an array of four pumps, where on each pump of the array, an autonomous and wireless 3D microsystem (called here "e-cube") is installed for real time monitoring of vibration, humidity, temperature and strain and wireless transmission of the "health data" to a central station (Fig. 1).

The electronic blocks of our 3D chip 'e-cube" (Fig. 2) consist of a set of sensors, power supply and its management, signal conditioning and analog to digital converter, followed by digital processing (microprocessor, memory) and RF transceiver block and its antenna.

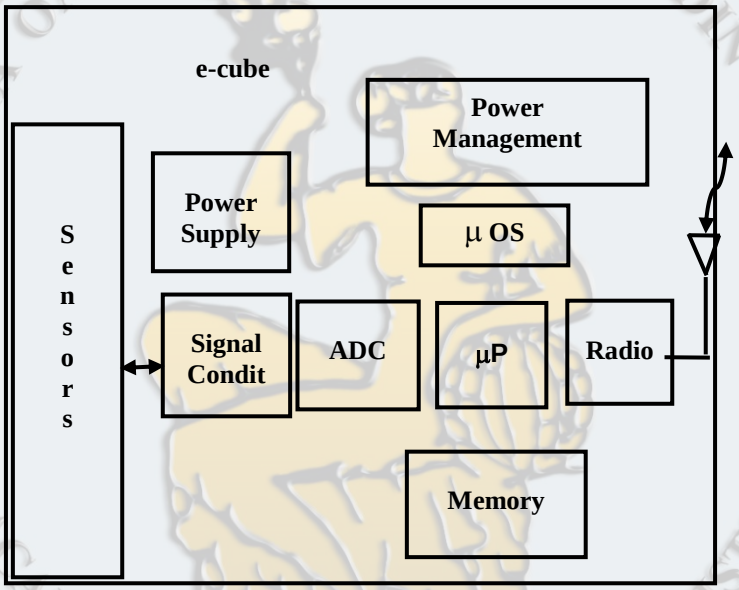

Fig. 2. Reduced Functionality Device (e-cube) containing the sensors and electronics.

Due to the limited hardware and software (H&S) resources of the autonomous 3D integrated Microsystem, specific to battery operated or energy harvested micro-systems, the e-cube is considered a Reduced Functionality Device, while the wireless electronic interrogator (Fig. 3) of the e-cube is having more H&S resources, being thus called Full Functional Device, and able to have a dialog with all four "e-cubes" and a higher capacity of data storage and management, in our example.

Our SHCMA application is operating by means of alarming thresholds for vibration, temperature, strain and even the battery life. The robust operation of our SHCMA application is based on understanding the operation of the pump components, and detailed studies of failure modes of these, with major focus on

the most susceptible-to-failure components like bearings, for example. For this SHCMA application, the vibration frequency spectra of the good and defective bearing are needed, as they become an important part of the decision regarding the health of the pump, and the appropriate actions of continuation or stopping the pump for maintenance purposes.

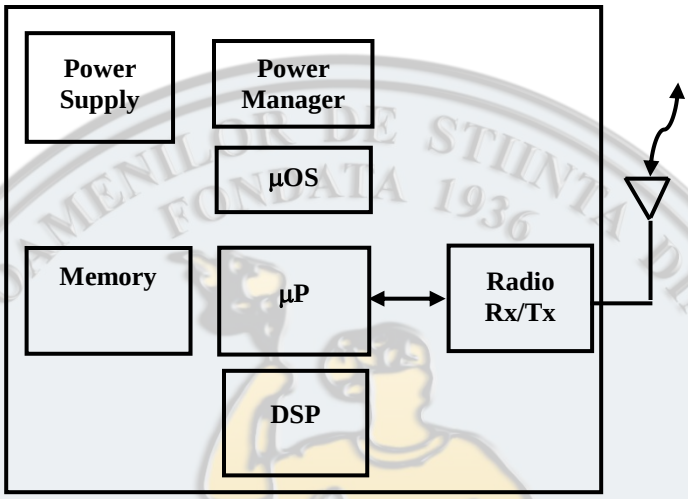

Fig. 3. Full Functionality Device used for the interrogation of e-cube.

It is shown in the literature [16] that based on the frequency domain analysis for a good bearing a poor vibration frequency spectrum is observed, with a dominant vibration component at 20 Hz, while for a defective bearing, one can note a very rich vibration spectrum with frequency components from 3 Hz to 260 Hz. From such a study, one can decide that the alarming level for defective bearing could be the appearance in the spectrum of the vibration frequency below 10 Hz.

A similar threshold approach should be pursuit for the interrogation of the health of each pump from the array as a function of the humidity, temperature and strain measured by each "e-cube".

The battery of the e-cube should be periodically interrogated for checking its voltage level. An example of monitoring strategy is presented in Fig. 4, where the logic diagram for SHCMA operating alarming in case of pump or e-cube malfunction is shown.

Going top-down with the brief description of our SHCMA application, we show below two different technological approaches for the realization of the sensing part and signal conditioning blocks of our e-cube for pump monitoring, as described above.

In the first technology solution [17], we present a rapid prototyping concept for 3D technology. For this "rapid" technology route, the 2D un-packaged chips for

sensors and signal conditioning are flip-chip mounted on the flexible tape provided with double side metallization and vias (Fig. 5).

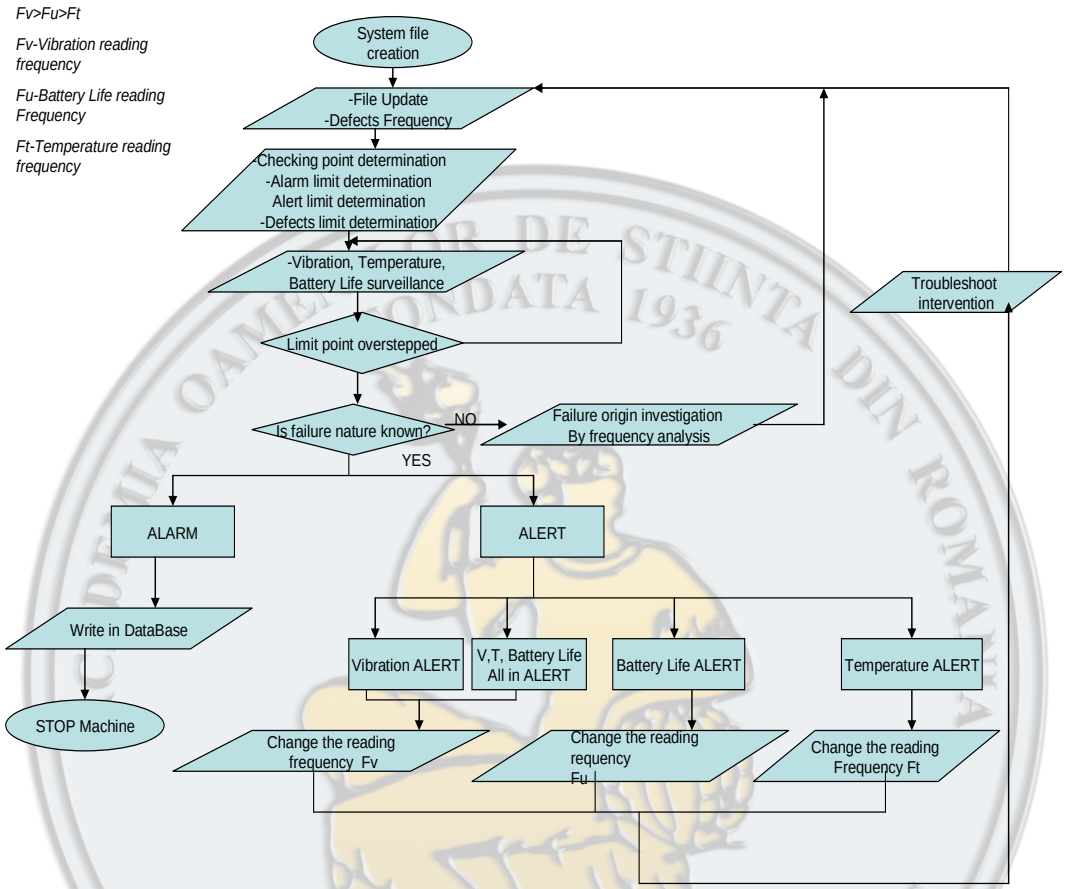

Fig. 4. Monitoring strategy performed by the 3D chip ("e-cube").

After mounting all the chips on the flexible tape, the folding step will follow, so that a final 3D stack is obtained as shown in Fig. 6, where the whole package for the sensing part of the e-cube is shown.

In the second generic technology solution [18], we present a genuine 3D technology approach, where the chips are processed as in the 2D technology and subsequently bonded in order to obtain the 3D stack, as shown in Fig. 7.

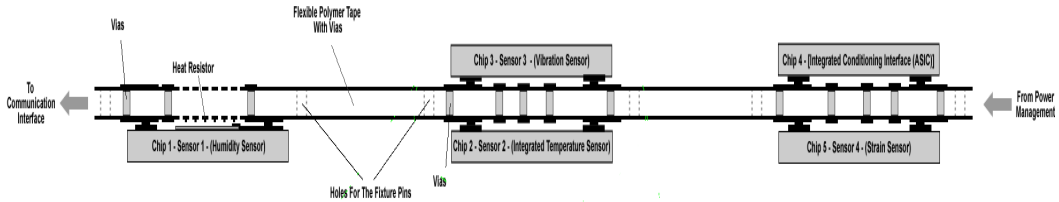

Fig. 5. Mounting the chips on the flexible tape.

This figure shows only the sensing chips and the chip for signal conditioning and processing, specific to sensor operation. In the 3D stack from Fig. 7, one can notice that the sensors for humidity and strain measurement should be positioned in the direct contact with the external ambience, while vibration and temperature sensor can be placed inside the 3D stack. Here the substrate thickness for each chip is much thinner than in the "classic" 2D technology, while through-the-chip vias are making the electrical and mechanical connection between the chips.

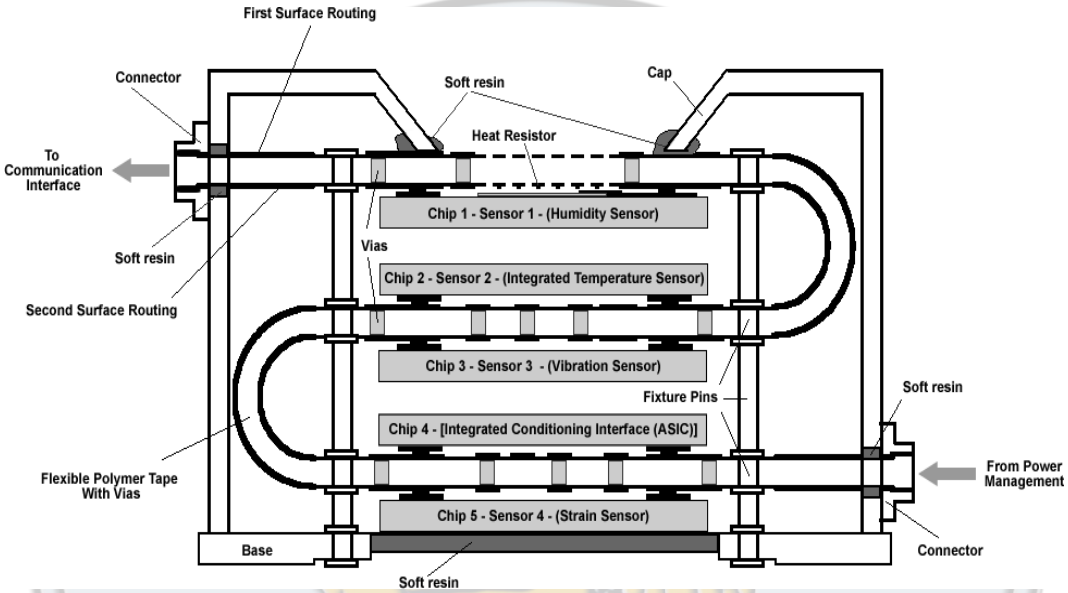

Fig. 6. Folding the tape for getting a 3D stack.

Virtual implementation of the above 3D technology is shown below, where all sensors specific to our SHCMA application from above are to be performed on quartz substrate (Fig. 8) and they use the dependence of the propagation velocity of the surface acoustic wave (SAW) devices, on the strain, temperature, mass loading as well as the changes of the electrical conductivity or dielectric constant of a layer deposited on the quartz surface (Fig. 8 a). For such SAW devices, the piezoelectric effect is intensively used for the generation of the acoustic waves from ac electrical signals and the conversion of the acoustic waves into ac electrical signals. Our application is using SAW delay line (DL) based sensors for the above measure and detection (Fig. 8b), where each DL has two interdigital transducers (IDT), and in between them there is a space used for sensing. The input IDT is converting the excitation ac electrical signal into acoustic waves, while the output IDT is converting the acoustic signal, carrying the sensing information into ac electrical signal.

In Fig. 8c, we show an intuitive example of a SAW sensor for acceleration/vibration measurement, where a diaphragm provided with an inertial mass is generating strain into that diaphragm when the sensor is exposed to an external acceleration.

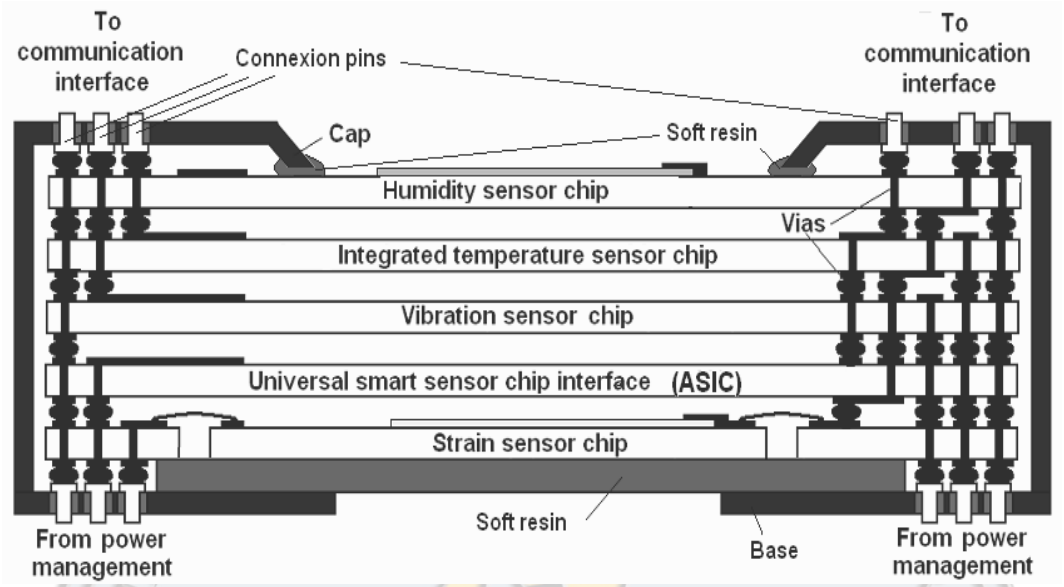

Fig. 7. Genuine 3D-MEMS Packaging solution.

The signal conditioning from the SAW delay line based sensors is shown in Fig. 9, where a multitude of SAW sensors are interrogated by the same electronic reader.

The propagation velocity of the acoustic waves in SAW resonators and SAW delay line is changing as a function of temperature, mass loading, external pressure/torque, changes in the conductivity or dielectric permittivity of a coating layer.

$$\frac{\Delta v}{v_o} = \frac{1}{v_o}\left(\frac{\partial v}{\partial m}\Delta m + \frac{\partial v}{\partial c}\Delta c + \frac{\partial v}{\partial \sigma}\Delta \sigma + \frac{\partial v}{\partial \varepsilon}\Delta \varepsilon + \frac{\partial v}{\partial T}\Delta T + \frac{\partial v}{\partial p}\Delta p + \ldots\right)$$

mass (m), stiffness (c), conductivity (σ), dielectric permittivity (ε), temperature (T), pressure (p)

Fig. 8.a

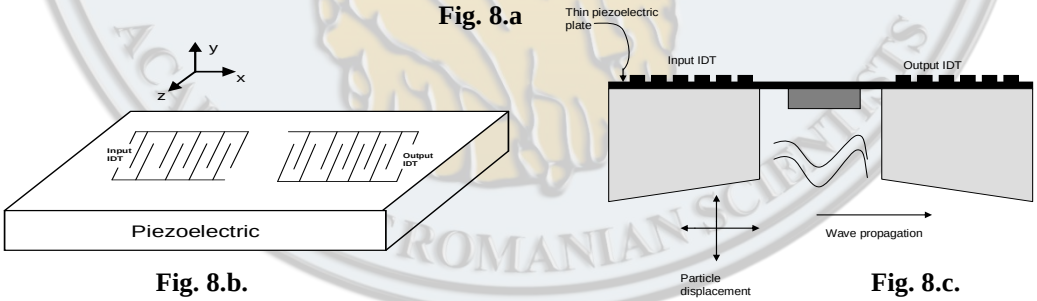

Fig. 8.b. **Fig. 8.c.**

Fig. 8. Surface Acoustic Wave Device to be used for sensing.

Thus, each sensor is interrogated, separately, by means of a multiplexer which is inserting that sensor in the feed-back loop of an oscillator. The external measurand is detected as a change in the oscillation frequency. The SAW sensors shown in Fig. 9 are processed separately on quartz substrate by a technology very similar to IC technology, and then stacking technology is used for the realization of the 3D approach.

In Fig. 10 (a), we show the sensing behavioral modeling at the system level, where the SAW delay line is placed in the feed-back loop of the above mentioned oscillator. In this figure, we show the electronic circuit schematic which was used, for modeling and simulation of the signal conditioning module from a SAW delay line sensor, while in the Fig. 10b, we show the start-up of the oscillation from such an oscillator with a SAW sensor in the feed-back loop.

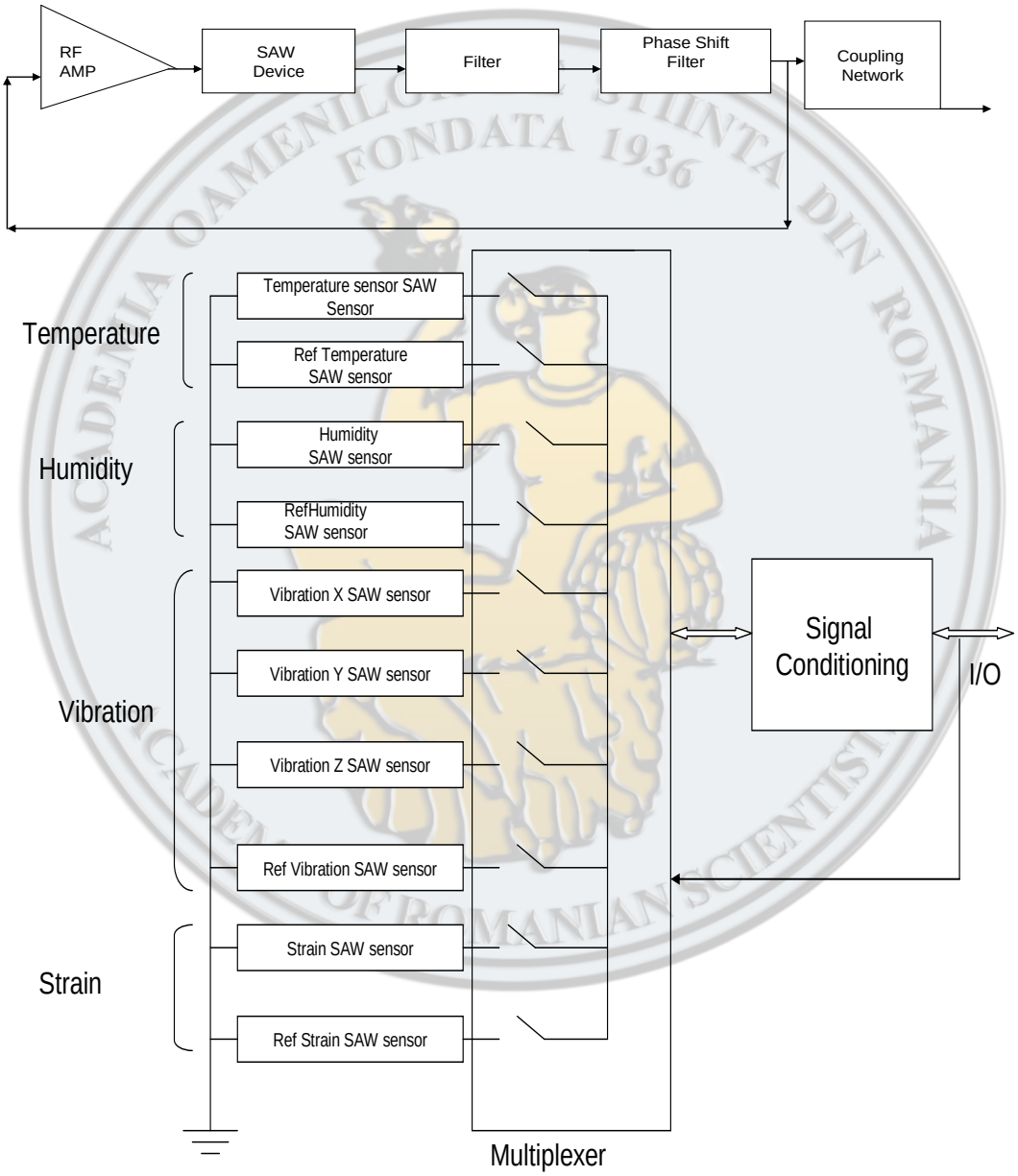

Fig. 9. SHCMA: Sensing Sub- e-CUBES description and signal conditioner.

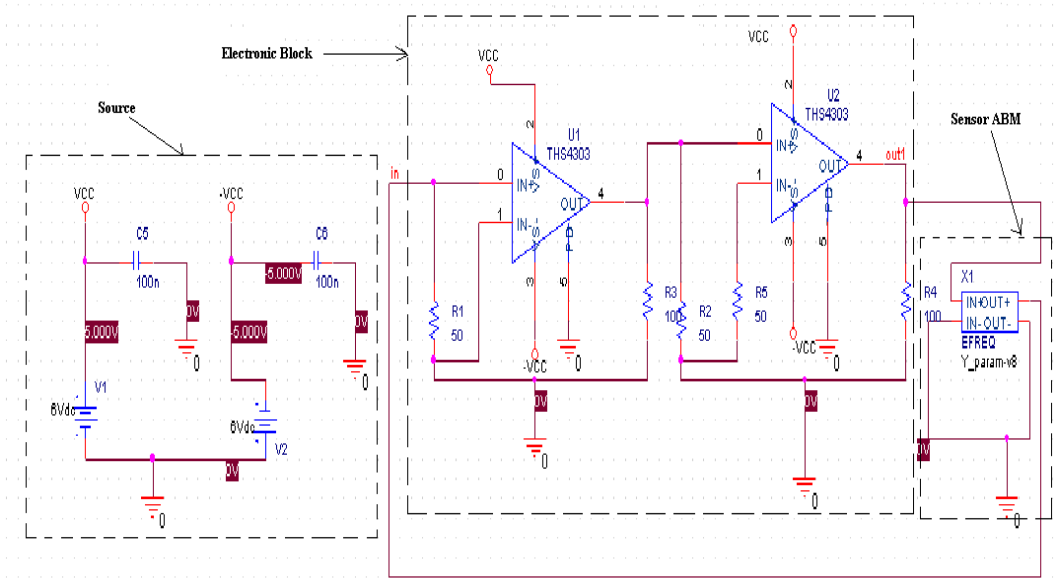

Fig. 10 (a). Electronic schematic of an oscillator with the SAW sensor in the feed-back loop.

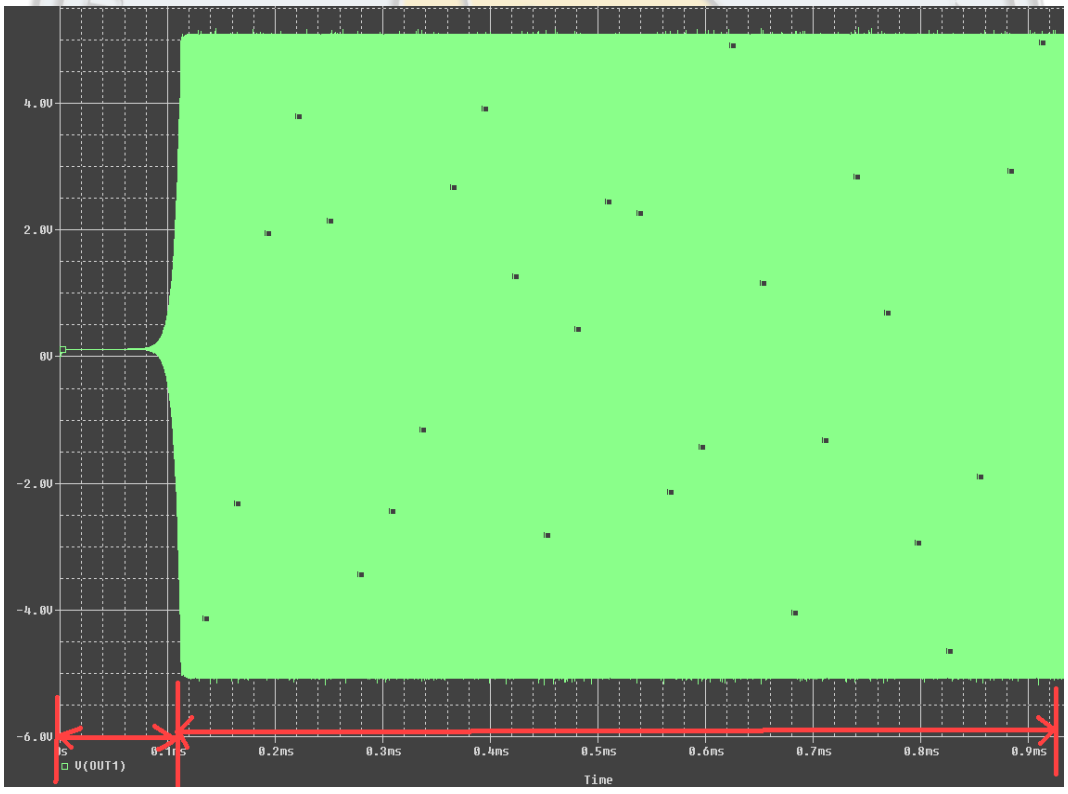

Fig. 10 (b). Start transient regime and steady state of the oscillation.

This is just a simple example of above virtual prototyping approach, which is the essential for predicting the functional performances of such wireless sensor systems.

This behavioral modeling is very important for reducing the cost of 3D MEMS micro systems due to the elimination of a great number of trials at the proof-of-concept level.

Finally, on can anticipate that beyond 2D "More Moore" technology, the emerging 3D "More Than Moore" technology is the only alternative to the present 2D hybrid IC system solutions and 2D SoC for complex applications for industrial process control, portable and consumer electronics applications, which are requiring high volume of data to be processed and wireless transmitted for a multifunctional control and operation.

Conclusions

This paper closes a huge loop between the vision of Moore on the 2D integrated electronics development and the emerging 3D technology which is developing these years, when 3D "More than Moore" is generating a viable market alternative to the well known 2D hybrid IC technology or 2D system-on-chip (SoC).

The paper recognizes Gordon Moore as the father of international technology roadmap for semiconductors, due to his capability to predict the evolution of the complexity of integrated 2D electronics for more than 4 decades, based on a limited amount of information available, in 1965.

In addition, the paper describes the 2D electronics challenges identified by Moore, in terms of integrated capacitors, inductors and developing high Q devices on silicon substrate and how the scientific community has started to solve them by considering 2D-MEMS and 3D MEMS technology, in what is called 3D "More than Moore" technology.

In the end, the paper presents examples of 3D packaging solutions developed by us for the realization of an industrial application that can be implemented by 3D-MEMS technology and wireless sensor network concepts.

The paper expresses the importance of behavioral modeling and simulation for the virtual prototyping of complex applications, such as structural health continuous monitoring of industrial assets, exemplified in this paper by an array of pumps.

This SHCMA application is a simple example for a big paradigm change in the field of real time monitoring systems based on wireless system network that will replace the schedule-based-maintenance by condition-based maintenance in the future industrial and home-med applications.

Acknowledgment

The authors would like to thanks Honeywell and European Union (project e-CUBES, EU-FP-6 program) for their support to develop this research.

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