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AN ACCURATE ANALYTICAL MODEL WITH A REDUCED PARAMETER SET FOR SHORT-CHANNEL MOS TRANSISTORS

Andrei SEVCENCO[1], Gheorghe BREZEANU[2]

Rezumat. *Este prezentat un model analitic compact, bazat pe numai câțiva parametri, pentru caracteristicile electrice ale tranzistorului MOS submicronic pentru a fi utilizat în proiectarea analogă. Efecte secundare, ca viteza de saturare și modularea lungimii canalului sunt incluse atât pentru dispozitivele nMOS cât și pentru cele pMOS. Sunt propuși noi parametri pentru descrierea vitezei efectului de saturație. Este demonstrată o aproximare liniară a dependenței vitezei purtătorilor de sarcină de câmpul electric. Este realizată o bună concordanță între model și datele experimentale pentru caracteristicile de transfer și de ieșire și pentru transconductanță, măsurate pe tranzistoare nMOS și pMOS standard (0,18 μm și 0,35 μm).*

Abstract. *A compact analytical model, based only on a few parameters, for the electrical characteristics of submicron MOS transistors to be used in analogue design is presented. Secondary effects like velocity saturation and channel length modulation are included in the model for both nMOS and pMOS devices. New parameters are proposed for the description of the velocity saturation effect. A linear approach of the dependence of the carrier velocity on the electric field is proved. A very good agreement between model and experimental data is achieved for transfer, output characteristics and transconductance measured on standard 0.18 and 0.35μm nMOS and pMOS transistors.*

Key words: MOS transistor, short channel, analytical model

1. Introduction

Technology advances have brought the microelectronic industry to never before seen levels of efficiency in production of ICs. This is a feat supported mainly by the extreme scaling of the most basic cell of electronic devices, the MOS transistor. This has not always been done in the best way needed. Since customer ease of use has always been a primordial condition for good business, in the beginning of the microelectronic industry as we know it today MOS devices were scaled through the constant voltage technique. This was due to TTL compatibility needs of the, then current, IC market. This in turn created very high fields in the channel of the MOS transistor, as channel lengths were ever smaller while voltages applied to these channels were always constant.

[1]University ”Politehnica” of Bucharest, Romania, andrei.sevcenco@catsemi.ro.
[2]University ”Politehnica” of Bucharest, Romania, gheorghe.brezeanu@dce.pub.ro.